On the Modeling of LDMOS RF Power Transistors

(Invited Paper)

John Wood and Peter H. Aaen
Freescale Semiconductor Inc., RF Division, Tempe, Arizona USA

***Abstract*— In this review we present a technology-independent approach to the construction of a circuit model for a high-power radio-frequency (RF) LDMOS FET. We compare and contrast this approach with other MOSFET modeling approaches used for digital and RF CMOS applications. We describe the structure of our model, the mathematical development of the constitutive relations, and the functions used for their approximation. This model is fully nonlinear, with a self-consistent dynamic electro-thermal component, and uses electromagnetic simulations to derive the on-die and in-package components that connect the transistor to the outside world. We also outline some of the characterization and validation measurement challenges that we have overcome in the development of this model.**

I. Introduction

Modern power amplifiers for wireless communications systems are tightly specified in terms of their linearity performance and bandwidth, while at the same time customers are requiring higher powers, and ever-higher efficiency. Several high-efficiency modes of operation have been investigated in recent years, including load-modulation, power-supply modulation, and harmonic terminations [1], with the Doherty amplifier becoming the architecture of choice in commercial base-station deployment. These amplifiers are designed to achieve a compromise between the RF power delivered, DC-to-RF conversion efficiency, and linearity. Successful design places a premium on the availability of accurate device models.

Base-station power amplifiers for wireless infrastructure use laterally-diffused MOS (LDMOS) FETs almost exclusively for the high-power transistors. These transistors provide an unmatchable combination of power and cost. In Fig. 1 we show examples of packaged high-power transistors, capable of delivering hundreds of watts of RF power. The complexity of the transistor in terms of the number of components in the package can be seen; much of this product is not the transistor die itself, but comprises the in-package matching components, bond-wires, and so on. These components, although linear, have a significant influence on the RF properties of the device, and need to be included in the complete model. In addition, the high-power operation of the transistor results in the generation and dissipation of considerable heat, therefore a self-consistent electro-thermal model is essential.

The active transistor die dominates the nonlinear behaviour of the device, and so the device model needs to capture these electrical properties accurately to be a satisfactory model for RF design. Several approaches to MOS FET modeling have been proposed and demonstrated in recent years. Physically-based models, such as BSIM, have been the mainstay of CMOS circuit design for many years. This approach has been extended to describe RF CMOS devices in BSIM5 [2]. A recent development in physically-based MOS modeling is the surface potential or PSP model, which uses the surface potential, rather than the threshold voltage, as a major control parameter [3]. This model has been used successfully for low frequency designs, and has extensions for RF applications. These various modeling approaches will be compared and contrasted with our approach in the next section.

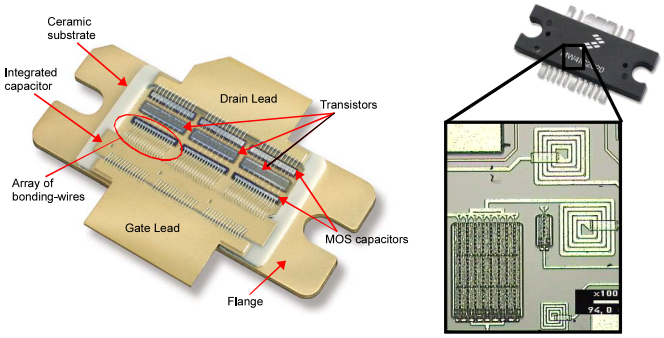

Fig. 1. Examples of LDMOS power transistors with views of the internal components. Bond-wires, spiral inductors, and other matching elements within the package are visible. These transistors are capable of delivering hundreds of watts of RF power at their 1-dB compression points.

In this paper we describe a method for the generation of a compact model of the power transistor that can be used in a circuit simulator for the design of RF power amplifiers. The model is derived directly from electrical measurements of the transistor, and so careful characterization is required. This presents a number of practical challenges in the measurements, which are described in Section III. A segmentation approach is used to define the reference planes at the active and passive components of the power transistor. The passive elements are determined from measurement and from electromagnetic simulations, outlined in Section IV. The nonlinear part of model is extracted directly from the bias-dependent network parameters determined at the intrinsic reference planes, and can thus be described as a measurement-based or technology-independent model. Our model construction preserves the dynamics and nonlinearities of the device. The details of the extraction of extrinsic and intrinsic parameters of the model are presented in Section V. The thermal modeling approach is described in Section VI, and includes threshold voltage shift as well as current degradation through a reduction in carrier mobility. Finally, we present some illustrative validation data, using measured data that has been taken in a different measurement environment from the one used for the model characterization.

II. MOSFET Modeling Approaches

The generally accepted approach to creating a compact model for a semiconductor device is to anchor the model firmly in the condensed-matter physics describing the behaviour of the semiconductors. This has proven to be successful with devices such as bipolar transistors, where relatively simple junction and carrier transport physics can describe the terminal electrical characteristics accurately. For field effect transistors, the semiconductor physics are significantly more involved. Originally, the physics of the Junction FET as developed by Shockley were applicable only up to the onset of the saturation region, and the description of charge transport in the saturation region was somewhat vague.

A great deal of effort and research have been invested in developing the physical description of the MOS transistor in the saturation region, based on Shockley's original model of the charge in the channel being determined by the gate voltage and the threshold voltage of the metal-oxide-silicon system. The drain current then depends on this charge, and the electric field-dependent charge (electron) mobility, which determines the charge carrier velocity in the inversion channel beneath the gate [4]. This led to the development of compact models based on the threshold voltage formulation, with the state of the art being the BSIM family [5], and the MOS Model 9 [6].

The BSIM3v3 model accommodates a number of other physical effects related to the structure of the MOS transistor, including: nonuniform doping in the channel; channel-length modulation; short channel effects; field-dependent mobility and velocity saturation; drain-induced barrier lowering effect (DIBL); impact ionization due to the high electric fields present; and depletion effects in polysilicon gates [5]. Later versions, BSIM4, account for new physical effects seen in advanced CMOS processes and at high levels of scaling. Such physical phenomena include: gate leakage due to tunneling effects [7], and quantization effects in the inversion layer [8]. The BSIM4 model also includes some extrinsic elements, which become important at high frequencies [9], and consequently this model is seeing application in RF CMOS IC design.

The MOS Model 9 was developed by deGraaff and Klaassen [6]; it uses the same charge density and electric field equations for the current and charge descriptions, resulting in a consistent approach. The authors also pay attention to the implementation of the model in the simulator in that these charge and current expressions are continuous and continuously differentiable. Weak and strong inversion regions are well described, as is the transition from the linear to the saturation regime.

As device scaling has become more aggressive, the threshold voltage-based approach has begun to show some deficiencies in its model description. For instance, as the supply voltage is reduced, the device spends a greater fraction of time in the moderate inversion region, the physics of which is better described by a surface-potential approach.

Surface-potential models have become more popular in the last decade or so, as techniques for computing the surface potential were developed. This approach uses a consistent physical description for all regions of the device operation. One model seeing wide adoption is the PSP model [3], which is the result of merging two compatible surface potential models: the SP model from Penn State University [10], and MOS Model 11 from Philips Electronics [11]. The PSP model comprises an intrinsic model of the channel region, describing the charge transport and quasi-static charge distributions, and an extrinsic model to account for the access resistances, overlap capacitances, substrate current, and so forth. The PSP model also includes descriptions of the physical effects seen in scaled, short-channel devices, as listed earlier, and also has a 'non-quasi-static' module that can account for the time delays in the channel charging behaviour, allowing for modeling of high-frequency effects. A related model is the EKV model [12]: this uses an inversion charge rather than surface potential as the controlling physical mechanism. The EKV model also describes many of the physical effects and structure-related behaviors outlined above, and has descriptions of charge sharing and non-quasi-static effects that are useful for high-frequency applications [13].

The main advantage of adopting a physically-based approach to modeling the transistor is the link between the device structure, material properties, and underlying physics, with the terminal electrical characteristics: a clear dependence of changing a physical feature on the electrical behavior can be seen. Some other potential advantages follow from the physically-based model too. For instance, the temperature dependences of the material properties can be included in a direct way in the model, with the electrical behavior then reflecting the thermal effects faithfully. Variations in the material properties or in the layers and structures of the transistor can also be included, as simple statistical variations or with practical joint probabilities, to create a statistically-based model for prediction of circuit performance over process variation.

This main advantage is also one of the main drawbacks with these physically-based models. The level of detailed physics and structural information that must be captured in the model results in a large number of equations to describe the device behavior, and leads to a similarly large number of parameters whose values need to determined from measurement or theory. The ramifications are twofold: first, the large number of equations that describe the model must be solved by the simulator many times as the simulation proceeds towards convergence. Additionally, their derivatives must be calculated for the Jacobian. These arithmetic calculations take time, and hence the simulations can be long, testing the patience of the circuit designer. Second, all of the parameter values must be extracted from careful measurements designed to isolate the various physical effects. This is a process that requires a skilled practitioner, and, again, some patience.

Our approach to compact modeling is derived from a different perspective from the CMOS IC world, and is informed by a number of environmental factors. First, the end application for the circuits designed using LDMOS transistors is RF power

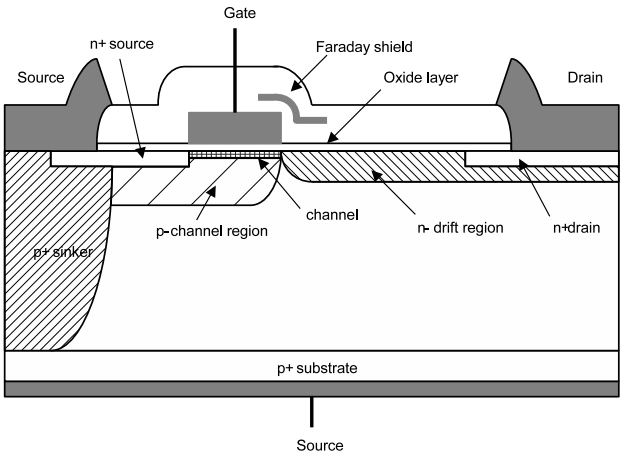

Fig. 2. Schematic cross-section of an LDMOS RF power transistor, showing the lightly-doped drift region and the inherent asymmetry of the device structure [14]. © 2007 Cambridge University Press. Reprinted with permission.

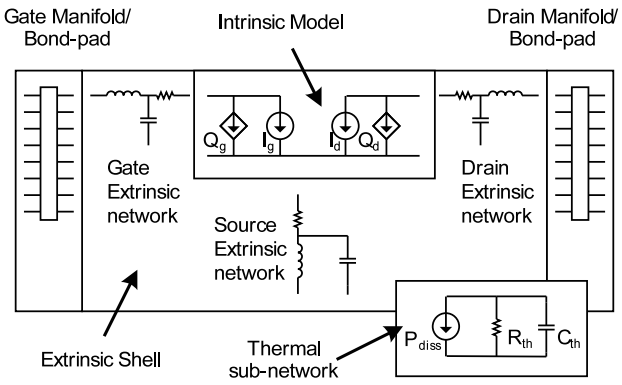

Fig. 3. A high-level view of the nonlinear model structure. The model can be thought of as a set of 'shells' comprising the gate and drain manifolds, the extrinsic network, the thermal model, and at the kernel, the intrinsic nonlinear model [16].

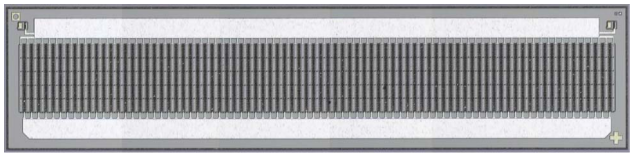

Fig. 4. A single die block of an LDMOS transistor. This die contains 164 gate fingers for a total gate width of 82 mm. The die is about 1 cm across. It is capable of producing about 80 W of RF power at 2 GHz. Photograph courtesy of Freescale Semiconductor, Inc.

amplifiers: the simulations for these designs are usually performed in the frequency-domain. Our main concerns are therefore with efficient simulation in harmonic-balance simulators, and accommodating non-quasi-static effects into the model structure from the outset, rather than as an additional feature. Second, the LDMOS power transistors, while fabricated in a CMOS process, have rather longer gate lengths than the state-of-the-art CMOS FETs, typically 0.3 – 0.5 μm, and do not currently exhibit many of the short gate effects that must be modeled for a CMOS design. A cross-section of a typical RF power LDMOS FET is shown in Fig. 2. It can be seen that this device is not symmetrical in structure, and some of the standard compact modeling paradigms therefore do not apply. Further, we have to be able to address several variants of a 'standard' LDMOS process to accommodate a broad product portfolio. These aspects mean that we need to be able to extract many models in a short time: a model with a large number of extractable parameters is not the most appropriate one, hence our pursuit of a technology-independent approach.

We have chosen to adopt a 'process-independent' modeling approach [14], in which the number of extractable parameters is relatively small, and these parameters can be extracted fairly directly from straightforward two-port network measurements at RF. This approach has been used successfully in other RF and microwave technologies, for deriving compact circuit model for GaAs FETs and HEMTs, for example [15]. The model is mapped onto the two-port network structure, whose values are given by the network parameters, which represent the transistor's constitutive equations. The model architecture is shown in Fig. 3, which identifies the main features of the LDMOS transistor that we need to include. In addition to the nonlinear kernel, there are extrinsic components – the access resistances, and inductance and capacitance of the metal lines contacting the gate and drain, which act as transmission lines at RF – and the large area manifolds for the gate and drain bond pads, which again introduce inductive and capacitive effects. These features can be seen in the photograph in Fig. 4, which shows a typical high-power LDMOS die.

III. Measurements and Model Extraction

Power transistors are large devices, expressed in terms of total gate width, and this presents a number of problems in measurement. First, the currents drawn can be quite high, leading to unacceptable self-heating in DC measurements as the device dissipates a lot of heat, and the channel temperature is not uniform over bias. This can result in a model whose parameters cannot be reconciled with a single operating temperature, making it difficult to implement in a meaningful manner. The large gate width means that the gate and drain impedances that the device presents at RF are very low. This can cause oscillation in a 50-Ω measurement system. The problems of high current demand and potential for oscillation generally place an upper limit on the transistor size for model characterization measurements. Even so, using transistors of up to 5 mm total gate periphery is not uncommon for LDMOS power transistor characterization. The characterization is normally carried out on-wafer, in a temperature-controlled environment.

Pulsed measurements are frequently used for the I-V and S-parameter characterization of power transistors for model extraction. Pulsed techniques offer a number of advantages over DC measurements. The energy input to the device is determined by the pulse width and the duty cycle, enabling the temperature of the transistor to be controlled. Effectively, we are de-coupling the thermal and electrical dependences

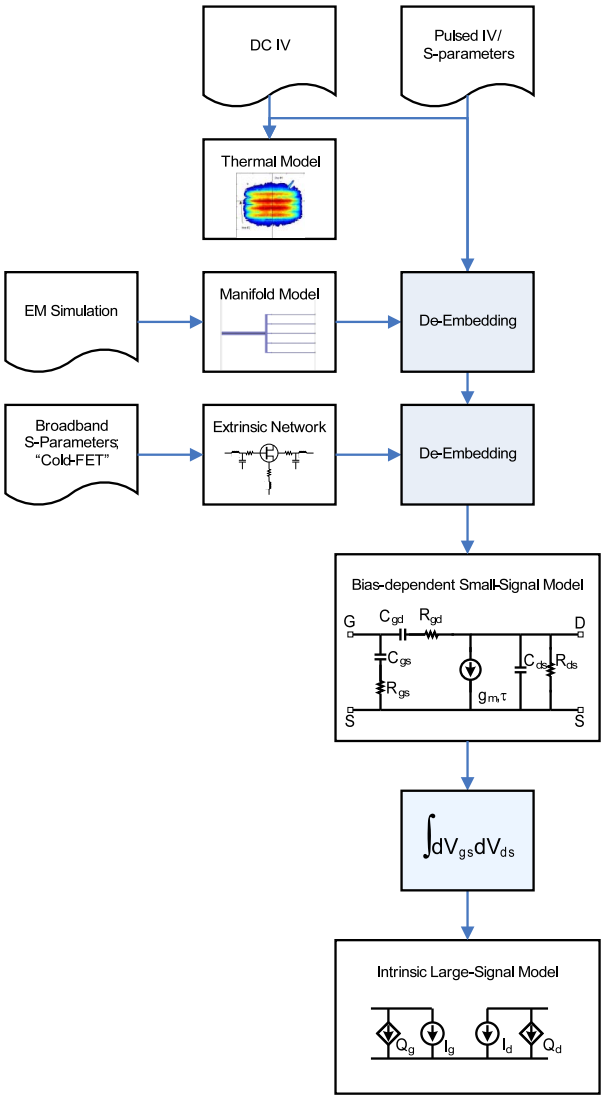

Fig. 5. A flowchart of the model extraction procedure: pulsed IV and S-parameter measurements, DC IV measurements, and broadband S-parameter measurements are made; the manifold metallizations are simulated using an EM simulator to get an S-parameter model; after de-embedding and integration over the bias voltage space, we obtain the large-signal model.

of the model parameters [14], [17], and enforcing isothermal conditions over the whole measurement set.

Using short time pulses also enables us to measure in regions of the output I-V characteristics that would otherwise be inaccessible under DC conditions, because of the thermal power dissipation limits or voltage breakdown limits that have a long relaxation time associated with them. This enables us to produce a model that can predict the device operation more accurately under real drive conditions, where the instantaneous or RF load-line trajectory lies beyond the DC limiting conditions.

The activity flow for the measurements and the model extraction algorithms is outlined in Fig. 5. We make pulsed I-V and S-parameters over a wide range of {Vgs, Vds} bias space, at a number of discrete frequencies. We make additional broadband S-parameter measurements under "Cold-FET" bias conditions to enable the extraction of the extrinsic network parameters, described in Section IV. The model extraction procedure is outlined in more detail below, and in [18], [19]. The procedure is largely independent of the device technology, provided the source connection is grounded (floating source models can be extracted, with a little extra difficulty): only the topology of the extrinsic network has any technology dependence, as it captures much of the device layout detail.

IV. The Package and In-package Components

The passive components that surround the LDMOS die provide an impedance transformation from the low impedances presented by the die to an impedance level that is easier to match on the amplifier circuit board. These in-package matching networks are usually composed of arrays of bond-wires and MOS capacitors, or integrated spiral inductors, capacitors and transmission line elements. In RF power amplifiers, the bond-wires are circuit elements, not parasitic connections.

Often we have several hundred bond-wires all in close proximity to one another within the package. The effects of coupling between individual wires and between arrays of wires must be included in the model. Through the development of segmentation procedures, it is possible to divide the entire packaged transistor into sub-sections, and to simulate the components in finite-element and method-of-moments based simulators. The results are then combined using network theory to generate the model of the matching networks [20]. Often, the manifold metallizations can be modeled as simple capacitors, but for more accurate models we rely upon electromagnetic simulations of the metal polygon, often including the bond-wire termination itself. The manifold can then be represented as a multi-port S-parameter network in the simulator [18].

The so-called extrinsic network represents the part of the transistor that is needed to connect the active channel region to the outside world. This includes: the resistive losses due to the access resistances between the source and gate electrodes and the channel; the inter-electrode capacitances; inductances of these metal electrodes, which can be several hundreds of microns long in a high power transistor. Several techniques have been described for identifying a suitable network, and for determining its parameter values [15], [21], [22]. Probably the most commonly used method is "Cold-FET": here the transistor is biased into a passive condition, with the drain bias at zero voltage, and the gate is biased below threshold so that the device is switched off. In this condition the intrinsic transistor can be modeled as a network of capacitors, enabling the extrinsic component values to be determined using broadband S-parameter measurements [22].

V. The Nonlinear Model

Referring back to the nonlinear kernel shown in Fig. 3, this intrinsic model is not defined by the device physics, but is determined directly from the RF network measurements: this is often called an empirical or measurement-based model. At

high frequencies we use S-parameters to describe the two-port relationships between the currents and voltages, which are measured in terms of magnitude and phase of the power waves at the two ports. The measured S-parameters are converted to Y-parameter description for the intrinsic model extraction. Before we get to this step, we must de-embed the manifolds and extrinsic parameter network, as shown in Fig. 5. By converting the measured S-parameters to Y-parameters, we obtain a small-signal two-port network description of the transistor at every bias point. It is convenient to re-cast the Y-parameter description in terms of circuit components such as capacitors and resistors, thus eliminating frequency from the measured data set. This data reduction creates a small-signal equivalent circuit model, parameterized by bias [14], [23].

Often, these bias-dependent small-signal circuit element values are fitted to a two-dimensional function of the gate and drain voltages, and expressed as a large-signal model. While such a model may operate in the simulator, it contains two-terminal capacitors whose instantaneous value is a function of two voltages: for example, the gate-source capacitor's charge is clearly controlled by the (time derivative of the) gate-to-source potential across its terminal, but it is more difficult to justify how the charge on this two-terminal capacitor can be changed by the drain voltage. This is an unphysical situation that defies the Law of Conservation of Charge, and which has been well-described by Snider [24], [25]; yet such components appear in many so-called large-signal models.

The correct way to convert this model into a non-quasi-static large signal model is to integrate the small signal capacitance values over the bias space, and enforcing conservation through the *curl* of the capacitance components to obtain a conservative charge field [14], [23], [26]. This derivative of this charge with respect to time describes the displacement current component of the gate and drain branch currents, is easily implemented in the simulator, and can be determined to be charge-conservative. The integral equations describing the gate and drain charges and currents in a non-quasi-static model are presented in (1)–(4).

Why is charge conservation so important? The circuit simulator will enforce current conservation in the way in which it solves the nodal admittance matrix equations to reach a convergent solution: Kirchhoff's Current and Voltage Laws are automatically implemented in the simulator solution method. In contrast, the simulator does not enforce any physical rules on the two-terminal components that make up the circuit: provided the models for the circuit elements return a current for an impressed voltage, the simulator will attempt to enforce Kirchhoff's Laws to arrive at a solution. Hence the difficulty with two-terminal components delivering a current that is controlled not only by the behavior of the voltage across its terminals, but also by some remote and physically unconnected voltage. In practical terms, when simulating with a large-signal frequency domain engine, if the path in the charge field that is described in one cycle of the voltage waveform does not end up at the same place it started, this means that charge is being created or destroyed. Over several cycles, this excess charge can result in non-convergence. This is the best you can hope for. In some, possibly many cases, the simulator may converge to a result, which is bound to be incorrect because of the creation of unphysical charges and hence potentials in the circuit. A charge-conservative model avoids these uncertainties by construction. The capacitance field is illustrated in Fig. 6.

In more practical terms, the main nonlinearity in the FET is the drain current. This function accounts for most of the harmonic and intermodulation effects in the model. The effects of the nonlinear dependence of the gate and drain charge sheets on the terminal voltages are relatively small, which is perhaps why they have been overlooked, or the incorrect implementations not caused any major problems in many applications. In the design of RF power amplifiers for wireless infrastructure applications, the predictions of nonlinear behavior can be crucial in the success of a given design. It has been shown that non-charge-conservative device models can result in several dBs of error in the prediction of intermodulation products and

$$Q_{\mathrm{g}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right)=\int_{V_{\mathrm{gs0}}}^{V_{\mathrm{gs}}}\left[C_{\mathrm{gs}}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)+C_{\mathrm{gd}}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)\right]dv_{\mathrm{gs}}-\int_{V_{\mathrm{ds0}}}^{V_{\mathrm{ds}}}C_{\mathrm{gd}}\left(V_{\mathrm{gs}},v_{\mathrm{ds}}\right)dv_{\mathrm{ds}}+Q_{\mathrm{g}}\left(V_{\mathrm{gs0}},V_{\mathrm{ds0}}\right) \tag{1}$$

$$Q_{\mathrm{d}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right)=\int_{V_{\mathrm{gs0}}}^{V_{\mathrm{gs}}}\left[C_{\mathrm{m}}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)-C_{\mathrm{gd}}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)\right]dv_{\mathrm{gs}}+\int_{V_{\mathrm{ds0}}}^{V_{\mathrm{ds}}}\left[C_{\mathrm{ds}}\left(V_{\mathrm{gs}},v_{\mathrm{ds}}\right)+C_{\mathrm{gd}}\left(V_{\mathrm{gs}},v_{\mathrm{ds}}\right)\right]dv_{\mathrm{ds}}+Q_{\mathrm{d}}\left(V_{\mathrm{gs0}},V_{\mathrm{ds0}}\right) \tag{2}$$

$$I_{\mathrm{g}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right)=\int_{V_{\mathrm{gs0}}}^{V_{\mathrm{gs}}}\mathrm{Re}\left\{y_{11}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)\right\}dv_{\mathrm{gs}}+\int_{V_{\mathrm{ds0}}}^{V_{\mathrm{ds}}}\mathrm{Re}\left\{y_{12}\left(V_{\mathrm{gs}},v_{\mathrm{ds}}\right)\right\}dv_{\mathrm{ds}}+I_{\mathrm{g}}\left(V_{\mathrm{gs0}},V_{\mathrm{ds0}}\right)=\int_{V_{\mathrm{gs0}}}^{V_{\mathrm{gs}}}g_{\mathrm{gs}}\left(v_{\mathrm{gs}},V_{\mathrm{ds}}0\right)dv_{\mathrm{gs}}+I_{\mathrm{g}}\left(V_{\mathrm{gs0}},V_{\mathrm{ds0}}\right) \tag{3}$$

$$I_{\mathrm{d}}\left(V_{\mathrm{gs}},V_{\mathrm{ds}}\right)=\int_{V_{\mathrm{gs0}}}^{V_{\mathrm{gs}}}g_{\mathrm{m}}\left(v_{\mathrm{gs}},V_{\mathrm{ds0}}\right)dv_{\mathrm{gs}}+\int_{V_{\mathrm{ds0}}}^{V_{\mathrm{ds}}}g_{\mathrm{ds}}\left(V_{\mathrm{gs}},v_{\mathrm{ds}}\right)dv_{\mathrm{ds}}+I_{\mathrm{d}}\left(V_{\mathrm{gs0}},V_{\mathrm{ds0}}\right) \tag{4}$$

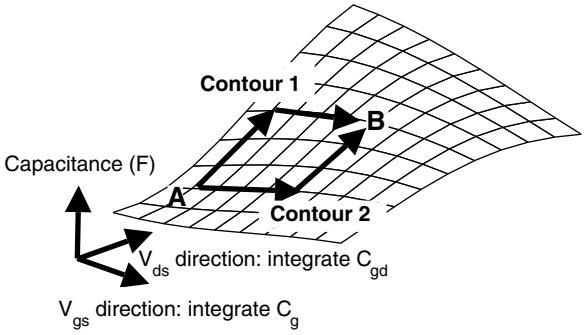

Fig. 6. A schematic of a two-dimensional capacitance field; points A and B represent the locations of two signal voltages in this field, and the two contours show different paths connecting them. The integral along any path from A to B yields the difference in charge. In a conservative system this must be independent of the path taken [14]. © 2007 Cambridge University Press. Reprinted with permission.

adjacent channel powers [27], which can lead to incorrect, or at least poorly-informed design choices.

After solving the integral equations we have the values of the gate and drain charges, and the drain current, at all combinations of the bias voltages {Vgs, Vds}. To build a useful model, we must find multivariate, differentiable functions that approximate these fields with sufficient accuracy. We can use elementary functions to do this; this process can take time and is dependent on the skill and experience of the modeling engineer, although this will often result in the most efficient model. As a practical alternative, we can use artificial neural networks as a general-purpose nonlinear function fitting method [28]. In each case, we must be concerned not only with the accuracy of the function fit to the data, but also the extrapolation qualities of the functions, their stability, and differentiability for forming the Jacobian [16].

VI. The Thermal Model

There are two main causes of temperature change in the transistor, defined as the difference in the instantaneous temperature in the device, and the temperature at which the model was extracted. The first is the change in the ambient temperature of the devices, and the second is the self-heating of the transistor due to the power dissipation in the FET, caused by the instantaneous current and voltage. The device model must be able to describe the effects on the terminal currents and voltages of these changes in temperature. This is especially important in power transistors, where the dissipated power, and hence self-heating, can be considerable, resulting in the device operating at a temperature substantially different from the one at which the model was originally determined: an accurate dynamical electro-thermal model must be built.

The thermal model needs to have a means of determining the instantaneous temperature. The ambient temperature can be a user-supplied input to the model in the simulation instance. The instantaneous temperature rise is often found using an auxiliary electrical network analogue of the thermal system, comprising a (thermal) resistance and capacitance network driven by a current source whose value represents the instantaneous power dissipation P_{diss}; the voltage across the network represents the temperature rise above ambient. This is described by the relationship:

$$\begin{aligned}\text{Heat Generation}(i_{\mathrm{d}}, v_{\mathrm{ds}}) = \text{Heat flow}(T_{rise}) \\ + \frac{d}{dt}(\text{Heat Storage})(T_{rise})\end{aligned}$$

which can be expressed as the following differential equation

$$P_{\mathrm{diss}}(t) = \frac{(T_{rise})}{R_{\mathrm{th}}} + C_{\mathrm{th}}\frac{d}{dt}\left(T_{rise}\right) \tag{5}$$

How we make use of this calculated temperature is determined by the structure of the model that we extract. In a physically-based model, the temperature dependences of all of the model parameters can be determined *a priori* from measurements made at several different temperatures, and then written into the model [17], in a manner assuring that the model is thermally consistent. While this approach has been widely applied, it can result in a model with a large number of thermal dependent parameters, which can lead to difficulties in parameter extraction, and potential convergence issues. A more pragmatic approach uses a de-rating function that is wrapped around the isothermal (pulsed) drain current expression, I_{d0}, [17], [29] and it can be expressed as:

$$I_{\mathrm{d}} = \frac{I_{\mathrm{d0}}}{1 + \dfrac{(T_{rise})}{T_0}} \tag{6}$$

where T_0 is the temperature at which the model was extracted. To complete the thermal model for an LDMOS transistor, we must also account for the variation with temperature of the threshold voltage. This acts in the opposite sense to the drain current de-rating, to produce a point in the drain current-gate voltage relationship that is independent of temperature: the zero-temperature coefficient point [30].

Several techniques are available to obtain the thermal resistance including direct measurement, indirect measurement, and simulation. Direct techniques measure the temperature at the top surface of the semiconductor die using infrared microscopy or alternatively through the application of temperature sensitive liquid crystals. To compute the thermal resistance we need to know the maximum temperature on the die, the temperature at the thermal reference plane and the amount of dissipated power. A thermocouple is placed in contact with the package and this temperature is captured. The dissipated power is computed as the product of the voltage and current at the drain (under DC operation), and R_{th} is computed by

$$R_{th} = \frac{\Delta T}{P_{diss}} \tag{7}$$

where ΔT is the temperature rise, and P_{diss} is the dissipated power (or incident heat-flux) [31]. Once the thermal resistance is known the thermal capacitance can be inferred from transient measurements.

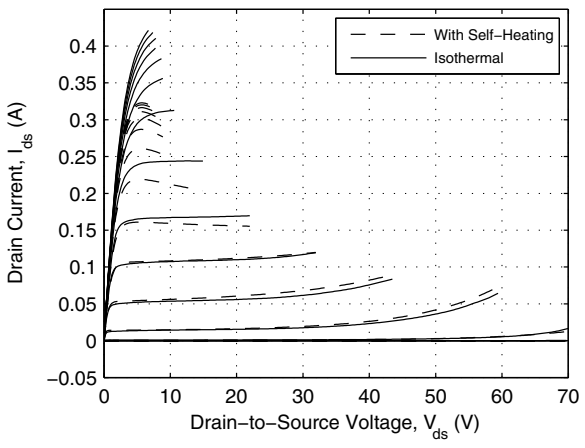

Fig. 7. Comparing the measured drain current under pulsed and continuous DC operation for a 2.4-mm LDMOS transistor. The continuous DC measurements show the degradation in drain current due to temperature.

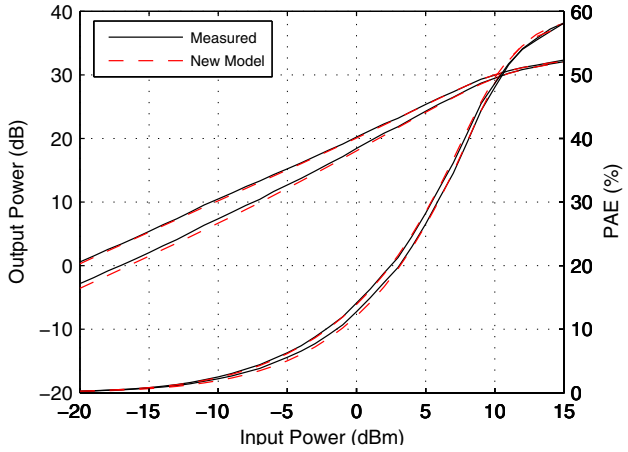

Fig. 8. Measued and modeled output power versus input power for bias currents equal to 6 and 9 mA/mm. (from [19])

Isothermal pulsed-IV measurements at an ambient temperature could also be collected and compared with DC-IV measurements. Where the drain current from the two measurement datasets match, we can infer the temperature and (7) can be used to compute the thermal resistance. Alternatively indirect measurements, or measurements of a temperature sensitive electrical parameter can be used, where we exploit the current-voltage relationship of a junction diode and its strong temperature dependence [32].

With this thermal model we are able to account for self-heating effects on the drain current as demonstrated in Fig. 7, where the device model is used to predict the changes in the drain current due to self-heating and under isothermal conditions.

VII. Implementation

In RF and microwave design, the circuit simulator must be able to describe distributed effects, transmission lines, coupling, and provide small-signal S-parameters as well as large signal power relationships, in the frequency domain, as this is the environment in which the RF amplifier is designed, built, and tested. The models must mimic the device behavior in this environment. The simulation tools are, accordingly, quite specialized.

We generally prototype the function fitting of the model's constitutive charge and current relations in a tool such as MATLAB®, to minimize the error while retaining flexibility to accommodate new processes, and keeping the parameter count relatively small. We have also used general-purpose nonlinear function fitting tools such as neural networks to generate the nonlinear models for the charge and current surfaces. After this step comes the prototype implementation in the target circuit simulator. We use the Symbolically-Defined Device (SDD) in Agilent's ADS, it is a well-established nonlinear modeling framework, which calculates the Jacobian numerically, thus enabling the model designer to focus on the implementation of the model equations. We also use Verilog-A as a prototyping vehicle; again this environment allows the modeler to focus on the model. The final implementation of the model is carried out in compiled code in the simulator, for the best speed performance. Compiling the model also protects intellectual property.

VIII. Model Validation

The first step in model validation is ensuring that the model as implemented performs the correct calculations and delivers the expected result: this is the '*Verification*' stage. Inputs giving known solutions are used to test the model implementation. We will also use the measured data that was used to extract the model, to see whether the model agrees to within some suitable accuracy. This is a necessary though not sufficient step in testing the fidelity of the model: we need to be able to do more than simply replicate the extraction measurements. To be useful in design, the model must be able to generalize, that is, predict behaviors that were not part of the original set of test vectors used in the model extraction. This is the purpose of '*Validation*.'

A typical suite of validation tests for an RF power transistor model would include: broadband S-parameter measurements under bias; swept power testing into compression, using one- and two-tone excitations to investigate the nonlinear predictions in harmonic balance simulation; load- and source-pull tests to ensure the transportability of the model, again, in harmonic balance. We present in Figs. 8 and 9 some typical large-signal validation results for our model.

IX. Conclusions

In this paper we have presented an approach to transistor modeling that is somewhat different from the physically-based modeling that is typically found supporting CMOS IC design. Our network-based modeling approach is more typical of that found in RF and microwave modeling, though we have tried here to outline a procedural approach to model generation. We have presented some of the measurement processes and analysis procedures that we believe should be followed in order to construct an accurate, mathematically correct model for a

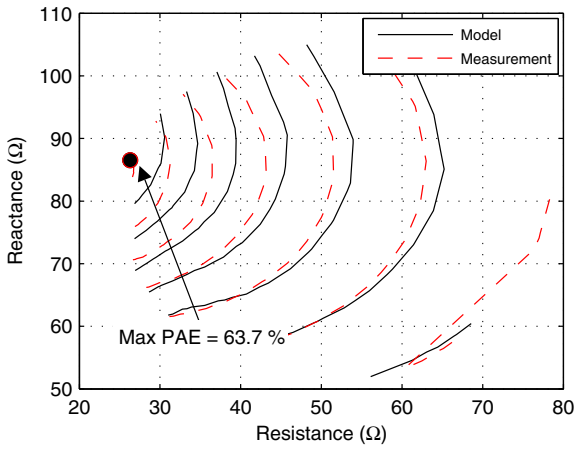

Fig. 9. Load-pull contours of power-added efficiency at P_{1dB}, comparing measured data and the model. The contours are spaced in steps of 4%. (from [19]).

power FET. We have described a charge-conservative approach to the extraction of the large-signal nonlinear model. We have also presented an elegant approach for the inclusion of a thermal model to produce a self-consistent, dynamic electro-thermal model that is suitable for use in power transistor circuit design. We have also presented a number of validation exercises for models of high-power RF transistors.

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