

A Pattern Matching-Based Framework for Quantum Circuit Rewriting

Hui Jiang, Diankang Li, Yuxin Deng, Ming Xu

Shanghai Key Laboratory of Trustworthy Computing, East China Normal University

Abstract. The realization of quantum algorithms relies on specific quantum compilations according to the underlying quantum processors. However, there are various ways to physically implement qubits in different physical devices and manipulate those qubits. These differences lead to different communication methods and connection topologies, with each vendor implementing its own set of primitive gates. Therefore, quantum circuits have to be rewritten or transformed in order to be transplanted from one platform to another. We propose a pattern matching-based framework for rewriting quantum circuits, called QRewriting. It takes advantage of a new representation of quantum circuits using symbol sequences. Unlike the traditional way of using directed acyclic graphs, the new representation allows us to easily identify the patterns that appear non-consecutively but reducible. Then, we convert the problem of pattern matching into that of finding distinct subsequences, and propose a polynomial-time dynamic programming-based pattern matching and replacement algorithm. We develop a rule library for basic optimizations and use it to rewrite the Arithmetic and Toffoli benchmarks from the G_{IBM} gate set to the G_{Sur} gate set. Compared with the existing tool PaF, QRewriting obtains an improvement of reducing depths (resp. gate counts) by 29% (resp. 14%).

1 Introduction

Quantum computing has attracted more and more interest in the last decades, since it provides the possibility to efficiently solve important problems such as integer factorization [28], unstructured search [8], and solving linear equations [9].

In recent years, with the popularity of quantum computing, many companies, universities and institutes are actively working to develop prototypes of quantum computer systems. For example, in 2019, Google announced the realization of quantum supremacy, the development of 53-qubit quantum processor “Sycamore” [3]. In November 2021, IBM unveiled its new 127-qubit “Eagle” processor whose scale makes it impossible for a classical computer to reliably simulate, and the increased qubit count allows users to explore problems at a new level of complexity [4]. In June 2022, Xanadu demonstrated a quantum computational advantage with a programmable photonic processor that realized Gaussian boson sampling on 216 squeezed modes [19]. These systems are referred to as Noisy Intermediate-Scale Quantum (NISQ) systems [26] and have small qubit

counts, restricted connectivity and high gate error rates. The coherence time of each physical qubit must be at least 1–10ns, if the minimum physical gate fidelity of 99% is to be achieved. At present, the duration of physical quantum gate is 10–100us and only a limited set of quantum gates can be realized with relatively high fidelity on a quantum device [15]. Each quantum processor may support a specific universal set of 1-qubit and 2-qubit gates, which are called primitive gates [16]. Table 1 lists three gate sets: G_{Com} , G_{IBM} and G_{Sur} , where G_{Com} is a universal gate set [23], G_{IBM} is implemented by the IBM QX5 quantum processor [7], and G_{Sur} is used by the Surface-17 quantum processor [17].

The realization of quantum algorithms relies on specific quantum compilations according to the underlying quantum processors. However, there are various ways to physically implement qubits in different physical devices and manipulate those qubits. These differences lead to different communication methods and connection topologies, with each vendor implementing its own set of primitive gates. Therefore, quantum circuits have to be transplanted or transplanted from one platform to another. In addition, since the gate types supported by a quantum processor is limited, quantum circuits may also be rewritten when some high-level gates are decomposed into low-level gates before the quantum circuits can be executed on the quantum processor.

Converting a quantum circuit supported by one gate set to a quantum circuit supported by another gate set with respect to some rules is called quantum circuit rewriting. Usually a rule is in the form $\mathcal{C}_p = \mathcal{C}_s$, where \mathcal{C}_p is a fragment of a circuit whose behaviour is the same as that of the fragment \mathcal{C}_s . We call \mathcal{C}_p a pattern circuit and \mathcal{C}_s a substitution circuit. In this paper, we refer to the circuit to be rewritten as the target circuit. Motivated by the aforementioned requirements, our approach consists of two key steps: one is to identify the desired patterns in the target circuit, the other is to replace them with semantically equivalent substitution circuits. For that purpose, we first introduce a new representation of quantum circuits using symbol sequences. Unlike the traditional way of using directed acyclic graphs (DAGs), the new representation allows us to easily identify the patterns that appear non-consecutively but reducible. In the case that a pattern can be matched by several different rules, we encounter a replacement conflict and need to resolve it with an appropriate policy. We propose three policies for generating schedulers to cope with the replacement conflicts. One policy is precise in the sense that it will consider all the replacement candidates of a conflict set. In the worst case, its time complexity is exponential. For a large-scale circuit, we need to make a trade-off between the quality of the generated circuit and the time it takes. Therefore, for large-scale circuits, we propose a greedy and a stochastic policy to handle the replacement conflicts.

The main contributions of this paper are listed below.

- We introduce a new representation of quantum circuits, which can easily identify the patterns that appear non-consecutively but remain reducible in the target circuits.
- We present a polynomial-time dynamic programming-based pattern matching and replacement algorithm.

Table 1: Gate sets used in our evaluation.

G_{Com} [23]	H, X, Y, Z, S, S^\dagger , T, T^\dagger , $R_z(\theta)$, CX
G_{IBM} [7]	$U1(\theta)$, $U2(\phi, \lambda)$, $U3(\theta, \phi, \lambda)$, CX
G_{Sur} [17]	X, Y, $R_x(\theta)$, $R_y(\theta)$, CZ

- We propose three policies for generating schedulers to deal with replacement conflicts.
- We develop a rule library for basic optimizations.

The rest of the paper is structured as follows. Section 2 introduces the related work. Section 3 recalls the preliminary notations about quantum computing. Section 4 proposes a new representation of quantum circuits. Section 5 discusses the design of the pattern matching-based quantum circuit rewriting framework. Section 6 shows two case studies. Section 7 evaluates QRewriting by using the BIGD [32], the Arithmetic and Toffoli [22] benchmarks. Finally, Section 8 provides the conclusion.

2 Related Work

Several quantum circuit optimization compilers have recently been proposed to compile a quantum circuit to various processors. For example, Qiskit [10] and t|ket> [29] support generic gate set; Quilc [30] is tailored for the Rigetti Agave quantum processor. There are several optimizers that automatically discover patterns [13, 14, 24, 33]. QRewriting aims to rewrite quantum circuits between different processors according to a given rule set, mainly focusing on pattern matching and replacement.

Pattern matching is widely used in circuit optimization. For example, many algorithms have employed peephole optimization and pattern matching to optimize circuits. Peephole optimization identifies small sets of instructions and replaces them with equivalent sets that have better performance [18, 20]. Exact matching is only feasible for small and medium-scale circuits [1]. Heuristics are often used in large-scale circuits, but they cannot ensure optimal results [11, 27]. In [25, 31], Prasad et al. and Soekens et al. showed how to find optimal quantum circuits for all 3-qubit functions. Nam et al. proposed five optimization subroutines [22]. Murali et al. developed the first multi-vendor quantum computer compiler which compiles from high-level languages to multiple real-system quantum computer prototypes, with device-specific optimizations [21]. The work of Chen et al. [6] is the closest to ours, where a quantum circuit optimization framework based on pattern matching (PaF) is proposed. It uses subgraph isomorphism to find a pattern circuit in the target quantum circuit according to a given external rule description, then replaces it with an equivalent one.

Previous work often treats a target circuit as a DAG, which is not able to identify the patterns that consist of several gates that appear non-consecutively.

In this paper, we introduce a new representation of quantum circuits, which can deal with non-consecutive patterns more conveniently. For quantum circuit rewriting, we propose a polynomial-time algorithm, which is based on dynamic programming to match and replace pattern circuits in the target circuit.

3 Preliminary

In this section, we introduce some notions and notations of quantum computing. Let \mathbb{Z} and \mathbb{C} denote the sets of all integers and complex numbers, respectively.

Classical information is stored in bits, while quantum information is stored in qubits. Besides two basic states $|0\rangle$ and $|1\rangle$, a qubit can be in any linear superposition state like $|\phi\rangle = a|0\rangle + b|1\rangle$, where $a, b \in \mathbb{C}$ satisfy the condition $|a|^2 + |b|^2 = 1$. The intuition is that $|\phi\rangle$ is in the state $|0\rangle$ with probability $|a|^2$ and in the state $|1\rangle$ with probability $|b|^2$.

A quantum gate acts on a collection of qubits, which are called the operation qubits of the gate. For example, the Hadamard gate (H gate) is applied on one qubit, and the CX gate is applied on two qubits. Its behaviour is described as:

$$\text{CX}(\alpha|0\rangle|\psi\rangle + \beta|1\rangle|\phi\rangle) = \alpha|0\rangle|\psi\rangle + \beta|1\rangle(X|\phi\rangle),$$

that is, we apply the X gate to the second qubit — called the *target* — if the first — the *control* — is in the state $|1\rangle$, and the identity transformation otherwise, where $|\psi\rangle$ and $|\phi\rangle$ are the state of the second qubit. Two other gates which are relevant include the 3-qubit Toffoli gate CCX and the doubly-controlled phase gate CCZ. Likewise, the CCX and CCZ gates apply X and Z gate, respectively, when the first two qubits are in state $|1\rangle$. Fig. 1 lists the symbols of some commonly used quantum gates.

In a quantum circuit each line represents a *wire*. The wire does not necessarily correspond to a physical wire, but may correspond to the passage of time or a physical particle that moves from one location to another through space. The interested reader can find more details of these gates from many textbooks such as [23]. The execution order of a quantum logical circuit is from left to right. The width of a quantum circuit refers to the number of qubits in the quantum circuit. The depth of a quantum circuit refers to the number of layers executable in parallel. We refer to a quantum circuit with depth less than 100 as a small-scale circuit, a quantum circuit with depth more than 1000 as a large-scale circuit, and the rest are medium-scale circuits.

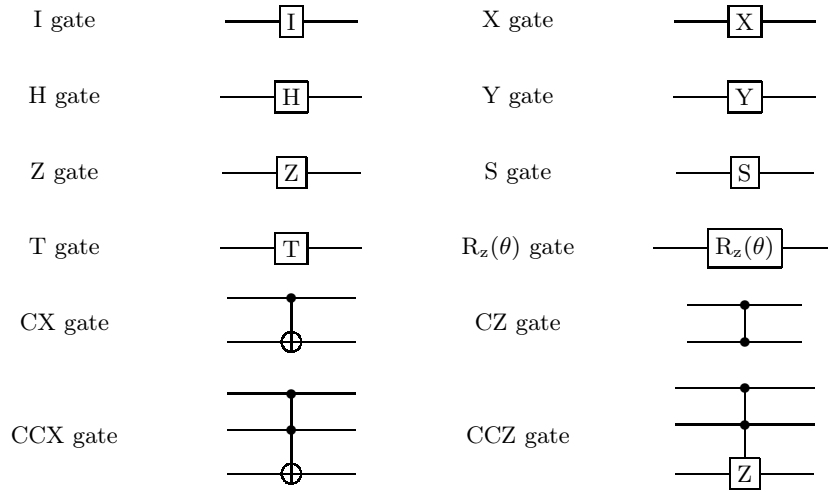


Fig. 1: Symbols of some commonly used quantum gates.

4 Circuit Representation

In this section, we define a new representation of quantum circuits and the pattern matching condition, which easily identifies the patterns that appear non-consecutively but are reducible. Based on that, we will state the quantum circuit rewriting problem considered in the paper.

Definition 1. *An instruction is represented by a triple (γ, ρ, α) , where*

- γ is the symbol of a gate type;
- ρ is a finite sequence of operation qubits for a gate;
- α is a finite sequence of rotation angles for a gate;

A quantum circuit \mathcal{C} is a sequence of triples $(\gamma_0, \rho_0, \alpha_0)(\gamma_1, \rho_1, \alpha_1) \cdots (\gamma_n, \rho_n, \alpha_n)$, and the length of the sequence is denoted by $|\mathcal{C}|$. The gate sequence $\Gamma_{\mathcal{C}}$ of the quantum circuit \mathcal{C} is a symbol sequence of gate types obtained by projecting each element of \mathcal{C} to its first component, e.g., $\Gamma_{\mathcal{C}} = \gamma_0 \gamma_1 \cdots \gamma_n$. The new representation of a rule is a pair $\mathcal{R} = (\mathcal{C}_p, \mathcal{C}_s)$, consisting of a pattern circuit \mathcal{C}_p and a substitution circuit \mathcal{C}_s . For simplicity, if the sequence is empty, we ignore it. Table 2 lists the gate symbols and the distinct aliases.

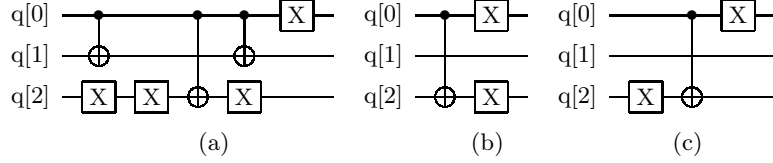
Example 1. Suppose we want to rewrite the quantum circuit \mathcal{C}_t in Fig. 2 (a). The new representation of the target quantum circuit \mathcal{C}_t is

$$- \mathcal{C}_t = ('x', [q[2]])(('x', [q[2]])(('c', [q[0], q[1]])(('c', [q[0], q[2]])(('c', [q[0], q[1]])(('x', [q[2]])(('x', [q[0]]),$$

and its gate sequence is represented by $\Gamma_t = \text{“xxcccx”}$. We can make use of the rule set $\{\mathcal{R}_1, \mathcal{R}_2, \mathcal{R}_3, \mathcal{R}_4\}$ in Fig. 3 to help with the circuit rewriting, where

Table 2: The symbols of gates and the distinct aliases.

Gates	Aliases	Gates	Aliases	Gates	Aliases	Gates	Aliases
I	'I'	H	'h'	X	'x'	Y	'y'
Z	'z'	T	't'	T^\dagger	'T'	S	's'
S^\dagger	'S'	R_x	'X'	R_y	'Y'	R_z	'Z'
CX	'c'	CZ	'C'	CCZ	'E'	CCX	'F'

Fig. 2: (a) The quantum circuit. (b) and (c) are the results of rewriting quantum circuit (a) using schedulers s_1 and s_2 , respectively.

- $\mathcal{R}_1 = ((\text{'x'}, [q[0]])(\text{'x'}, [q[0]]), (\text{'I'}, [q[0]]))$;
- $\mathcal{R}_2 = ((\text{'c'}, [q[0], q[1]])(\text{'c'}, [q[0], q[1]]), (\text{'I'}, [q[0]])(\text{'I'}, [q[1]]))$;
- $\mathcal{R}_3 = ((\text{'c'}, [q[0], q[1]])(\text{'c'}, [q[1], q[2]])(\text{'c'}, [q[0], q[1]]), (\text{'c'}, [q[0], q[2]])$
 $(\text{'c'}, [q[1], q[2]]))$;
- $\mathcal{R}_4 = ((\text{'x'}, [q[1]])(\text{'c'}, [q[0], q[1]])(\text{'x'}, [q[1]]), (\text{'c'}, [q[0], q[1]]))$;

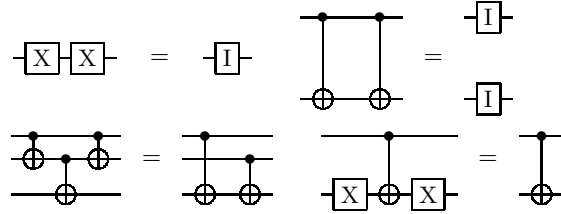


Fig. 3: The rules used to optimize the X and CX gates.

To facilitate the description of pattern matching, we introduce the following definition.

Definition 2. Let Γ and Γ' be two sequences. We say Γ' is a subsequence of Γ , if there exist indices $0 \leq i_0 < \dots < i_{|\Gamma'|-1} \leq |\Gamma|$ such that $\Gamma[i_k] = \Gamma'[k]$ for all $k \in [0, |\Gamma'|-1]$.

The subsequence set is a set of distinct subsequences of the pattern circuit in the target circuit. Note that we do not distinguish the indices from the gates

to which the indices correspond in the quantum circuit. Suppose Γ is a gate sequence. Then $\Gamma[a : b]$ means to take the segment of Γ from index a to b in, if b is not specified, we mean to take the suffix of Γ from index a . Suppose that s is a subsequence of Γ , we write $\Gamma \setminus s$ to mean the subsequence of Γ obtained by removing all occurrences of s .

Example 2. In Example 1, the gate sequences and its subsequence sets of the pattern circuits in the rule set are given as follows.

- “xx”: $\{\{0, 1\}\}$;
- “cc”: $\{\{2, 4\}\}$;
- “ccc”: $\{\}$;
- “xcx”: $\{\{1, 3, 5\}\}$.

Definition 3. (*Qubit mapping*) Given two qubit sets Q and Q' , a qubit mapping function f is a bijective function between the qubit sets Q and Q' .

Definition 4. (*Qubit state independence*) Let C_t, C_p be two circuits with gate sequences Γ_t, Γ_p , respectively. Suppose a subsequence $s = \{i_0, \dots, i_l\}$ of Γ_t that can match Γ_p . We say the qubit state in s is independent w.r.t. $\Gamma_t[i_0 : i_l] \setminus s$, if the control qubit set in s does not intersect with the target qubit set of the gates in $\Gamma_t[i_0 : i_l] \setminus s$, and vice-versa.

Definition 5. (*Pattern matching*) Let C_t and C_p be a target circuit and a pattern circuit with gate sequences Γ_t, Γ_p , respectively. We say C_p matches C_t if the following two conditions hold:

- Γ_t has a subsequence that can match Γ_p up to a qubit mapping;
- the qubit sets of the subsequence and the pattern circuit satisfy the qubit mapping and the qubit state independence conditions.

Example 3. We continue the last example to show the difference between the new representation of quantum circuits and the DAG representation. Suppose the instructions of circuit C_t (resp. pattern circuit of \mathcal{R}_2) from left to right are named g_0 – g_6 (resp. g'_0 – g'_1). In Fig. 4, (a) is the DAG representation of the circuit segment g_2 – g_4 and (b) is the DAG representation of the pattern circuit of \mathcal{R}_2 . We can intuitively see that (a) has no subgraph isomorphic to (b). But the pattern circuit of \mathcal{R}_2 matches the instructions g_2 and g_4 . It satisfies the qubit mapping function $\{f(q[0]) = q[0], f(q[1]) = q[1]\}$ and the qubit state independence condition. Therefore, the circuit C_t can be rewritten into $(\text{'x'}, [q[2]])(\text{'x'}, [q[2]])(\text{'c'}, [q[0], q[2]])(\text{'x'}, [q[2]])(\text{'x'}, [q[0]])$.

Definition 6. For a given target circuit C_t and a rule $\mathcal{R} = (C_p, C_s)$, a replacement candidate is a triple (s, p, c) , where

- s is a subsequence set of the target circuit C_t that can match the pattern circuit C_p ;
- p is a rule \mathcal{R} ;

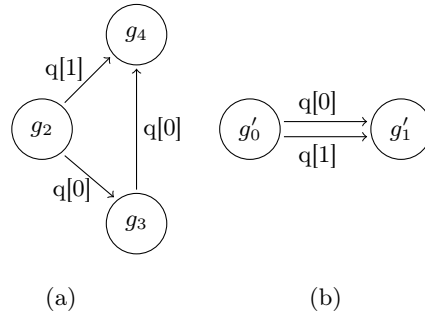


Fig. 4: (a) and (b) are the DAG representations of the circuit segment g_2 – g_4 of \mathcal{C} and the pattern circuit of \mathcal{R}_2 , respectively.

– $c \in \mathbb{Z}$ is a conflict index, with the default value being -1 .

Definition 7. A target circuit has a replacement conflict if an index of the target circuit appears more than once in the subsequence set.

The replacement candidates for a replacement conflict form a conflict set. A replacement scheduler is a set of replacement candidates for different indices.

Example 4. Continuing the last example, we see that the subsequence set of the sequence “cc” is $\{\{2, 4\}\}$, which appears non-consecutively in the sequence Γ_t . The first instruction (‘x’, $[q[2]]$) appears in both the subsequence sets of “xx” and “xcx”, which means that in the target circuit different rules may be matched at the same index. Two schedulers are given as follows.

- $s_1: \{(\{0, 1\}, \mathcal{R}_1, 1), (\{2, 4\}, \mathcal{R}_2)\}$,
- $s_2: \{(\{1, 3, 5\}, \mathcal{R}_4, 1), (\{2, 4\}, \mathcal{R}_2)\}$.

The scheduler s_1 (resp. s_2) replaces the instructions in the index set $\{0, 1\}$ (resp. $\{1, 3, 5\}$) using the substitution circuit of \mathcal{R}_1 (resp. \mathcal{R}_4). After one of the schedulers is applied, we obtain the circuit in Figs. 2 (b) or (c). Different schedulers result in different gate counts or depths of the rewritten circuits. The circuits \mathcal{C}_t rewritten using schedulers s_1 or s_2 have the same gate count but their depths are 2 and 3 respectively. In both schedulers, the first element has the component 1, which is an index to indicate where the conflict takes place.

We are now ready to state the following problem.

Problem 1. Given two gate sets G_1, G_2 and a rule set that expresses the equivalence of G_1 by the elements of G_2 , how to rewrite a quantum circuit supported by gate set G_1 to a quantum circuit supported by G_2 ?

By using our new representation of quantum circuits, we reduce the above problem to finding distinct subsequences of the pattern sequence in the target sequence up to a qubit mapping function and we use a qubit state independence condition to filter the obtained subsequences.

5 Quantum Circuit Rewriting

We propose a pattern matching-based quantum circuit rewriting framework. It consists of two steps. One matches the pattern circuit in the target circuit, the other replaces it.

5.1 Pattern Matching Algorithm

We propose an algorithm based on dynamic programming to match the patterns in a rule set against a target circuit. Let \mathcal{C}_t and \mathcal{C}_p be the target and pattern circuits with gate sequences Γ_t and Γ_p , respectively. We consider the problem of finding the distinct subsequences of the pattern sequence Γ_p in the target sequence Γ_t . The obtained subsequences only match the gate types, so we also need to check whether the operation qubits in the subsequences satisfy the qubit mapping function and qubit state independence condition.

The input of Algorithm 1 is a target circuit \mathcal{C}_t and a rule set \mathcal{R} , and the output is a set of replacement candidates \mathcal{M} . The function $distinct_subsequence(\Gamma_t, \Gamma_p, \delta)$ uses a dynamic programming algorithm to compute the distinct subsequences of Γ_t that can match Γ_p and returns the subsequence set to \mathcal{D} . The function $check_qubit_condition(\mathcal{D}, \mathcal{C}_t, p)$ checks whether the results in \mathcal{D} satisfy the qubit mapping function and qubit state independence condition.

The input of the function $distinct_subsequence(\Gamma_t, \Gamma_p, \delta)$ is a target sequence Γ_t , a pattern sequence Γ_p , and a parameter δ to limit the range of indices of Γ_p in Γ_t . The symbol $s[0]$ denotes the first component of the replacement candidate s . The output is a set $D[m+1]$ recording the distinct subsequences of Γ_t that can match Γ_p . We use the set $D[j+1]$ to record the subsequences of Γ_t that can match $\Gamma_p[0:j]$. If the condition $\Gamma_t[i] = \Gamma_p[j]$ is satisfied, there are subsequences of $\Gamma_t[0:i]$ that can match $\Gamma_p[0:j]$. Line 8 updates the set $D[j+1]$. To find the subsequence of $\Gamma_p[0:j]$, we need to first calculate the subsequences of $\Gamma_p[0:j-1]$. The update $D[j+1] \leftarrow D[j+1] \cup \{s \cup \{i\} : s \in D[j] \text{ and } j - s[0] < \delta\}$ is the Bellman equation [5], which is a necessary enabler of the dynamic programming algorithm.

The time complexity of Algorithm 1 is $\mathcal{O}(kmn)$, where k is the number of rules in the rule set \mathcal{R} , m is the maximum length of the gate sequence Γ_p in the rule set \mathcal{R} , and n is the length of the gate sequence Γ_t . The space complexity is $\mathcal{O}(m)$.

Example 5. Let us consider the quantum circuit in Fig. 10 (a) and the rule set $\mathcal{R} = \{\mathcal{R}_1, \mathcal{R}_2, \mathcal{R}_3, \mathcal{R}_4\}$ in Fig. 3. The gate sequences of the target circuit and the pattern circuits are “xxxxcccxcccxxxxcccxcccxxxxcccxccc”, “xx”, “cc”, “ccc”, and “xcx”, respectively. The set of subsequences of “cc” is as follows.

$$- \{\{4, 5\}, \{4, 6\}, \{5, 6\}, \dots\}.$$

The corresponding instructions of the indices $\{4, 5, 6\}$ in the target circuit \mathcal{C}_t are (‘c’, [q[13], q[2]])(‘c’, [q[9], q[14]])(‘c’, [q[4], q[12]]). The subsequences $\{4, 5\}$,

Algorithm 1: *pattern_matching*($\mathcal{C}_t, \mathcal{R}$)

Input: a quantum circuit \mathcal{C}_t and a rule set \mathcal{R} ;
Output: a set of substitution candidate \mathcal{M} ;

- 1 $\mathcal{M} \leftarrow \emptyset$;
- 2 $\Gamma_t \leftarrow$ the gate sequence of circuit \mathcal{C}_t ;
- 3 **foreach** $p \in \mathcal{R}$ **do**
- 4 $\Gamma_p \leftarrow$ the gate sequence of pattern circuit of p ;
- 5 $\mathcal{D} \leftarrow distinct_subsequence(\Gamma_t, \Gamma_p, \delta)$;
- 6 **if** *check_qubit_condition*($\mathcal{D}, \mathcal{C}_t, p$) **then**
- 7 $\mathcal{M} \leftarrow \mathcal{M} \cup \{(\mathcal{D}, p, -1)\}$;
- 8 **return** \mathcal{M} ;

Algorithm 2: *distinct_subsequence*($\Gamma_t, \Gamma_p, \delta$) (Bellman [5])

Input: two sequences Γ_t and Γ_p , and a parameter δ ;
Output: a set of subsequences of Γ_p ;

- 1 $n \leftarrow$ the length of Γ_t ;
- 2 $m \leftarrow$ the length of Γ_p ;
- 3 let D be an array of length $m + 1$;
- 4 $D[0] \leftarrow \emptyset$;
- 5 **for** $i \leftarrow 0$ **to** n **do**
- 6 **for** $j \leftarrow \min(i, m)$ **to** 0 **do**
- 7 **if** $\Gamma_t[i] = \Gamma_p[j]$ **then**
- 8 $D[j + 1] \leftarrow D[j + 1] \cup \{s \cup \{i\} : s \in D[j] \text{ and } j - s[0] < \delta\}$;
- 9 **return** $D[m + 1]$;

$\{4, 6\}$, $\{5, 6\}$ do not satisfy the qubit mapping function condition. We use the function *check_qubit_condition*() to filter the subsequences and finally get the subsequence set of “cc” in the gate sequence of the target circuit, which is $\{\{5, 12\}, \{19, 25\}\}$ highlighted with dotted lines in Fig. 10 (a).

5.2 Replacement Algorithm

By Algorithm 1, we obtain all the subsequences of the pattern circuits in the target circuit. To resolve replacement conflicts, we propose three conflict resolution policies. They give rise to three variants of QRewriting called QPRewriting, QGRewriting, and QSRewriting, respectively. Due to the decoherence of qubits, the lifetime of qubits is very short [34]. The execution time of the quantum circuit is determined by several factors such as the depth and the gate count of the quantum circuit. Here, we mainly use the depth to select the optimal replacement scheduler.

- Precise policy calculates all the candidates when a replacement conflict occurs.

- Greedy policy follows the principle “first come, first served”. That is, it chooses the one that appears first in the target circuit among the conflict set.
- Stochastic policy selects a candidate stochastically in the conflict set for the scheduler.

Algorithm 3: solve_conflicts(Γ_t, \mathcal{M})

Input: a gate sequence Γ_t and a set of replacement candidates \mathcal{M} ;
Output: a replacement scheduler;

```

1  $\mathcal{S} \leftarrow \emptyset$ ;
2 let  $Q$  be a scheduler queue;
3  $Q.push(\{\{\}, \epsilon, -1\})$ ;
4 while  $Q$  is not empty do
5    $s \leftarrow Q.pop()$ ;
6    $i \leftarrow next\_conflict(\Gamma_t, \mathcal{M}, s)$ ;
7   if  $i$  is None then
8      $\mathcal{S} \leftarrow \mathcal{S} \cup \{s\}$ ;
9     continue;
10   $\mathcal{N} \leftarrow$  Compute the conflict set on index  $i$ ;
11  foreach  $c \in \mathcal{N}$  do
12     $s \leftarrow s \cup \{c\}$ ;
13     $Q.push(s)$ ;
14 return compute_depth( $\mathcal{S}$ );
```

We propose an algorithm based on the breadth-first search to compute the replacement scheduler as shown in Algorithm 3. The input is a gate sequence Γ_t and a set of replacement candidates \mathcal{M} . \mathcal{S} is a scheduler set, and the queue Q stores the sub-scheduler. Firstly, we push one element $\{\{\}, \epsilon, -1\}$ into Q . Then, we loop the queue Q until it is empty in lines 4–13. The function $next_conflict(\Gamma_t, \mathcal{M}, s)$ computes the next conflict index i in Γ_t from the current conflict index to the end of Γ_t . If there is no conflict at this index, we directly add it to s , otherwise return the index. When arriving at the end of Γ_t , we add the scheduler s into \mathcal{S} . Line 10, according to the conflict policy, calculates the candidate set that has a conflict at index i in \mathcal{M} . Lines 11–13 append the replacement candidates to s and push it into queue Q . Finally, we calculate the depth of the replaced circuit and return the scheduler with the smallest depth.

The time complexity depends on the conflict policy. In the worst case, the precise policy is used and the time complexity is $\mathcal{O}(n^m)$, where m is the number of conflicts and n is the size of the conflict set. When dealing with large-scale circuits, the precise policy is not scalable. Therefore we do not show the precise policy in our experiments. The time complexity of both greedy and stochastic policies is $\mathcal{O}(mn)$.

Example 6. Let us continue the last example, where we show an example of generating schedulers. Starting from the index $i = 0$, we search for the next conflicting index i in \mathcal{M} . When $i = 18$, the conflict set is $\{(\{10, 18\}, \mathcal{R}_1, 18), (\{18, 26, 31\}, \mathcal{R}_4, 18)\}$. If the precise policy is used, we append the scheduler s with the two candidates and put into the queue Q , respectively, and the generated schedulers are given as follows.

$$\begin{array}{ll}
 s_1: & s_2: \\
 (\{0, 22\}, \mathcal{R}_1) & (\{0, 22\}, \mathcal{R}_1) \\
 (\{2, 13, 17\}, \mathcal{R}_4) & (\{2, 13, 17\}, \mathcal{R}_4) \\
 (\{3, 9\}, \mathcal{R}_1) & (\{3, 9\}, \mathcal{R}_1) \\
 (\{5, 12\}, \mathcal{R}_2) & (\{5, 12\}, \mathcal{R}_2) \\
 (\{10, 18\}, \mathcal{R}_1, 18) & (\{18, 26, 31\}, \mathcal{R}_4, 18) \\
 (\{15, 23\}, \mathcal{R}_1) & (\{15, 23\}, \mathcal{R}_1) \\
 (\{16, 24\}, \mathcal{R}_1) & (\{16, 24\}, \mathcal{R}_1) \\
 (\{19, 25\}, \mathcal{R}_2) & (\{19, 25\}, \mathcal{R}_2)
 \end{array}$$

If we use the greedy policy, the replacement candidate $(\{10, 18\}, \mathcal{R}_1, 18)$ will be selected, and the generated scheduler is s_1 . If we use the stochastic policy, one of them is selected and the finally generated scheduler is either s_1 or s_2 .

Algorithm 4 inputs a target circuit \mathcal{C}_t and a scheduler \mathcal{S} , and outputs a replaced circuit. We reversely traverse each element of the scheduler \mathcal{S} . Line 2 obtains the mapping relationship $qmaps$ of qubits between the subsequence of the target circuit and the pattern circuit, according to the qubit mapping function $qubits_mapping(\mathcal{S}[i])$. Lines 6–11 update the instructions on the target circuit with the substitution circuit one by one. If the substitution gate sequence is longer than the pattern gate sequence, the redundant gates are inserted after the index where the pattern circuit appears in the target circuit. Lines 10–11 remove redundant locations for the target circuit. The time complexity is $\mathcal{O}(mn)$, where n is the length of the scheduler, and m is the maximum length of the pattern circuit.

Example 7. Continuing the last example, we consider the replacement candidate $\mathcal{S}[i] = (\{2, 13, 17\}, \mathcal{R}_4)$ as an example. We can have that

$$\begin{array}{l}
 - \mathcal{R}_4 = ((\text{'x'}, [q[0]])(\text{'c'}, [q[0], q[1]])(\text{'x'}, [q[1]]), (\text{'c'}, [q[0], q[1]])); \\
 - qmaps = \{f(q[0]) = q[3], f(q[1]) = q[8]\}.
 \end{array}$$

The length of the pattern circuit is greater than that of the substitution circuit. First, we get $n = 1$ and update the second instruction of the target circuit \mathcal{C}_t with the instruction $(\text{'c'}, [q[3], q[8]])$. Then we remove the 13th and 17th instructions of the target circuit.

5.3 Quantum Circuit Optimization

We develop a rule library for basic optimizations. To facilitate the distinction between internally optimized rules and circuit rewriting rules, we divide the library into an internal library and an external one. The external library is a

Algorithm 4: substitute($\mathcal{C}_t, \mathcal{S}$)

Input: a quantum circuit \mathcal{C}_t , and a substitution scheduler \mathcal{S} ;
Output: the substituted circuit \mathcal{C}_t ;

```

1 for  $i \leftarrow \text{length}(\mathcal{S})-1$  to 0 do
2    $qmaps \leftarrow \text{qubits\_mapping}(\mathcal{S}[i]);$ 
3    $l_1 \leftarrow$  the length of the pattern circuit of  $\mathcal{S}[i]$ ;
4    $l_2 \leftarrow$  the length of the substitution circuit of  $\mathcal{S}[i]$ ;
5    $n \leftarrow \min(l_1, l_2);$ 
6   for  $j \leftarrow 0$  to  $n-1$  do
7      $\mathcal{C}_t.\text{update}(\mathcal{S}[i], j, qmaps);$ 
8   if  $l_2 > n$  then
9      $\mathcal{C}_t.\text{insert\_gate}(\mathcal{S}[i], qmaps, n);$ 
10  if  $l_1 > n$  then
11     $\mathcal{C}_t.\text{delete\_gate}(\mathcal{S}[i], n);$ 
12 return  $\mathcal{C}_t;$ 

```

rule set provided by a user, which can be a rule library for optimization or rewriting. The internal library is mainly used for basic reduction and quantum gate exchange [12, 22]. Note that almost all the gates implemented by quantum hardware devices are usually 1-qubit and 2-qubit gates, so our rule library mainly concerns 1-qubit gates and 2-qubit gates. The maximum input scale involved in the rule set is 3-qubit. The gate specification involves some cancellation rules for 1-qubit gates and 2-qubit gates, as shown in Fig. 5. The commutation rules shown in Fig. 6 include the transformation rules given in [12].

It is possible that after a step of circuit rewriting the target circuit still matches some rules. We repeat several rounds of internal optimization and circuit rewriting until no pattern circuit can be matched or the specified repetition bound is reached (5 by default in practice).

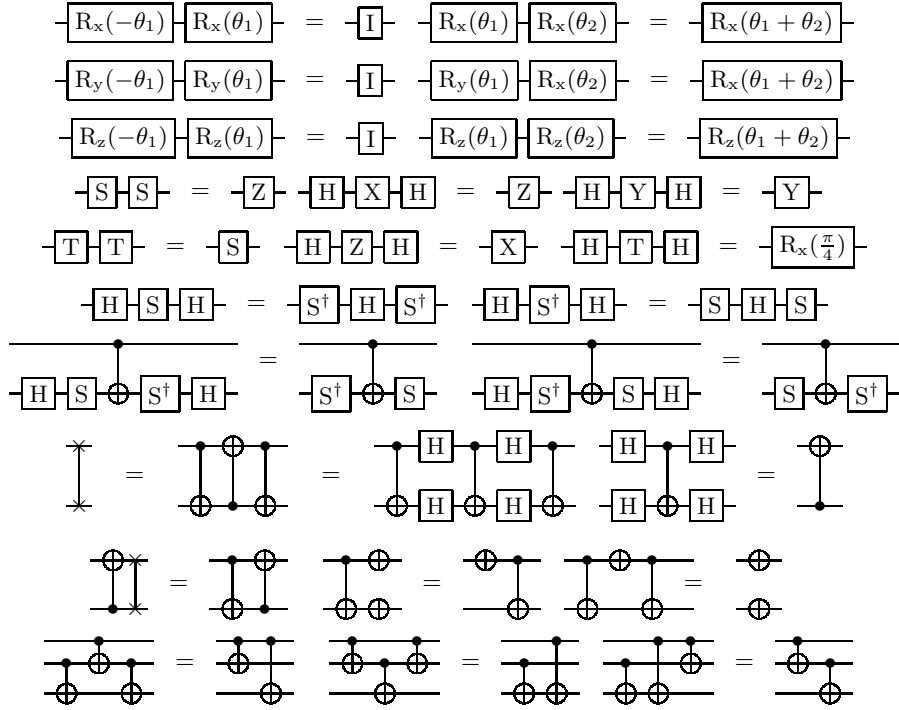


Fig. 5: The 1-qubit gate and 2-qubit gate cancellation rules.

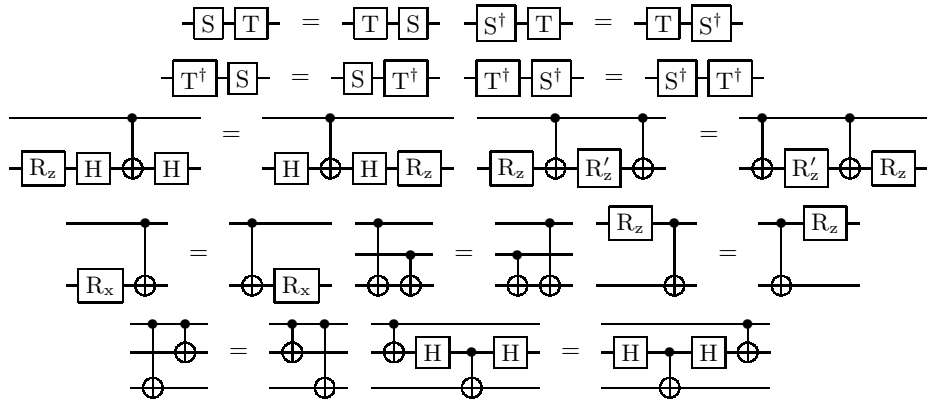


Fig. 6: The commutation gate rules.

6 Case Study

In this section we consider two examples: one rewrites a circuit with three CCZ gates to a circuit using the G_{Sur} gate set; the other optimizes a circuit with a stochastic policy.

6.1 Rewriting Circuits for Surface-17

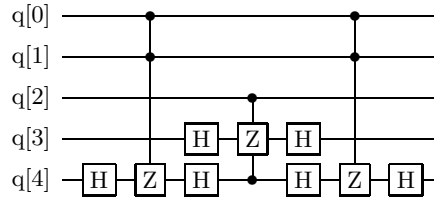


Fig. 7: The quantum circuit Toff-NC₃.

We demonstrate the use of QRewriting to rewrite the quantum circuit TOF_3 [32] that has three occurrences of the CCZ gates to the G_{Sur} gate set [17]. The target circuit $\mathcal{C}_t = ('h', [q[4]])(‘E’, [q[0], q[1], q[4]]) \dots$ is displayed in Fig. 7, and the rules are listed in Fig. 8. The CCZ gate decomposition rule [2] $\mathcal{R} = (\mathcal{C}_p, \mathcal{C}_s)$ is a pair, where

- $\mathcal{C}_p = ('E', [q[0], q[1], q[2]])$;
- $\mathcal{C}_s = ('t', [q[0]])('t', [q[1]]) \dots$

The gate sequence of the target circuit and the decomposition pattern circuit are “hEhhEhhEh” and “E”, respectively. The subsequence set of \mathcal{C}_t that can match “E” is $\{\{1\}, \{4\}, \{7\}\}$. Finally, the resulting circuit is shown in Fig. 9.

6.2 Optimization with a Stochastic Policy

Next we show an example of circuit optimization using QSRewriting with a stochastic policy. The target circuit and a set of rules $\mathcal{R} = \{\mathcal{R}_1, \mathcal{R}_2, \mathcal{R}_3, \mathcal{R}_4\}$ are shown in Fig. 10 (a) and Fig. 3, respectively. The gate sequences of the target circuit and the pattern circuits are “xxxxcccxcccccccccccccccccccc”, “xx”, “cc”, “ccc” and “xcx”, respectively. The subsequence sets of the gate sequence of pattern circuits are given as follows,

- “xx”: $\{\{3, 9\}, \{10, 18\}, \{0, 22\}, \{15, 23\}, \{16, 24\}\}$;
- “cc”: $\{\{5, 12\}, \{19, 25\}\}$;
- “ccc”: $\{\}$;
- “xcx”: $\{\{2, 13, 17\}, \{18, 26, 31\}\}$.

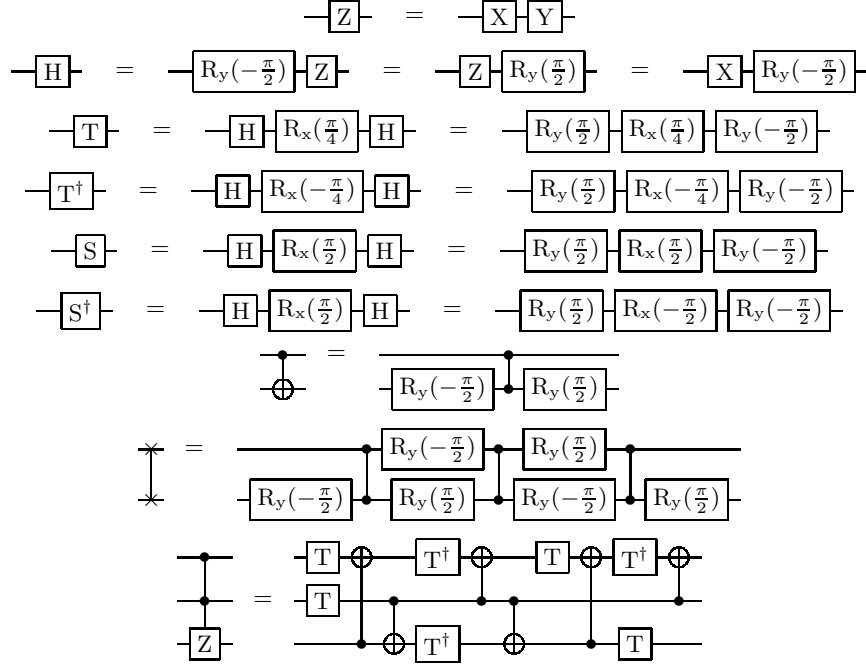


Fig 8: Gate decomposition into primitives supported in the superconducting Surface-17 processor.

The replacement candidates ($\{10, 18\}$, \mathcal{R}_1 , 18) and ($\{18, 26, 31\}$, \mathcal{R}_4 , 18) have a conflict at the index 18 of the target circuit. With the stochastic policy, either of the candidates can be chosen. Suppose the former is taken, then the generated replacement scheduler is given as follows.

s_1 :

- ($\{0, 22\}$, \mathcal{R}_1)
- ($\{2, 13, 17\}$, \mathcal{R}_4)
- ($\{3, 9\}$, \mathcal{R}_1)
- ($\{5, 12\}$, \mathcal{R}_2)
- ($\{10, 18\}$, \mathcal{R}_1 , 18)
- ($\{15, 23\}$, \mathcal{R}_1)
- ($\{16, 24\}$, \mathcal{R}_1)
- ($\{19, 25\}$, \mathcal{R}_2)

Finally, we obtain the resulting circuit in Fig. 10 (b), which reduces the gate count and the depth by 48.65% and 20%, respectively.

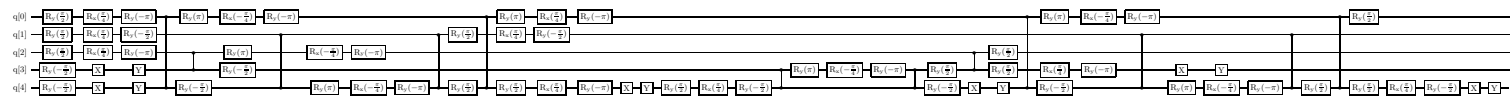


Fig. 9: The quantum circuit Toff-NC₃ rewritten to Surface-17 quantum processor.

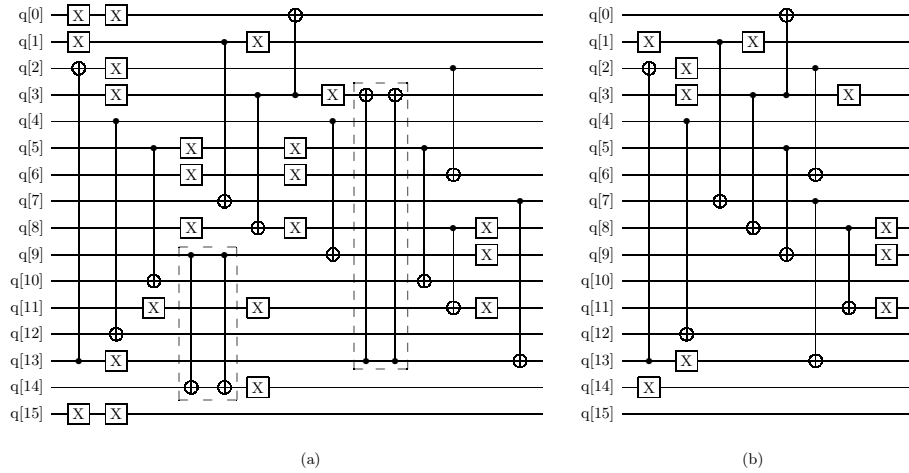


Fig. 10: (a) The quantum circuit 16QBT_05YCTFL_3. (b) The quantum circuit 16QBT_05YCTFL_3 optimized by QSRewriting.

7 Experiments

We compare QRewriting with the state-of-the-art algorithm for quantum circuit optimization framework based on pattern matching, namely PaF [6]. Notice that PaF is not freely available, so we implemented that algorithm in Python. The implementation of QRewriting in Python is available at <https://github.com/ShepherdLee519/qcpm.git>. All the experiments are conducted on a Ubuntu machine with a 2.2GHz CPU and 64G memory. For the stochastic policy, we execute QSRewriting five times and take the best result; for other policies the executions are deterministic, so we execute them only once.

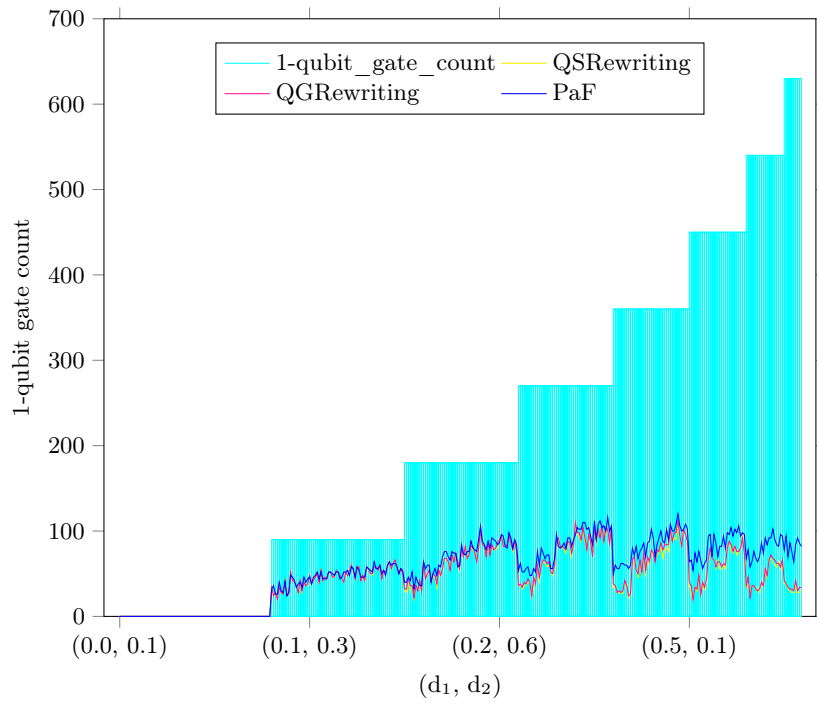
To compare with PaF, we adopt the BIGD benchmarks [32], and use the rule set shown in Fig. 3. We use the gate count and the depth as our evaluation metrics. The selected benchmarks are characterized by the parameters (d_1, d_2) , which is called gate density vector [32]. The two components stand for the densities of 1-qubit and 2-qubit gates in a benchmark. Suppose a quantum circuit has n qubits, M_1 (resp. M_2) is the number of 1-qubit (resp. 2-qubit) gates, and the longest dependency chain is l , then $d_1 = M_1/(n \times l)$ and $d_2 = 2 \times M_2/(n \times l)$.

The BIGD benchmarks include 360 circuits with a total number of 129600 gates. After a PaF optimization, the gate count and the depth decrease by 66512 and 4009 within 6760 seconds. QSRewriting (resp. QGRewriting) takes 2816 (resp. 1982) seconds to rewrite these circuits, and the resulting circuits further reduce the 1-qubit gate, 2-qubit gates, total gate count and depth by 18.7% (resp. 16.5%), 13.9% (resp. 12.8%), 14.6% (resp. 13.2%), and 29.0% (resp. 26.2%) compared with PaF. Therefore, QRewriting is about three times faster than PaF, and the resulting circuits are better optimized. The main evaluation results are shown in Fig. 10 (a)–(d) which compare the performance of QSRewriting,

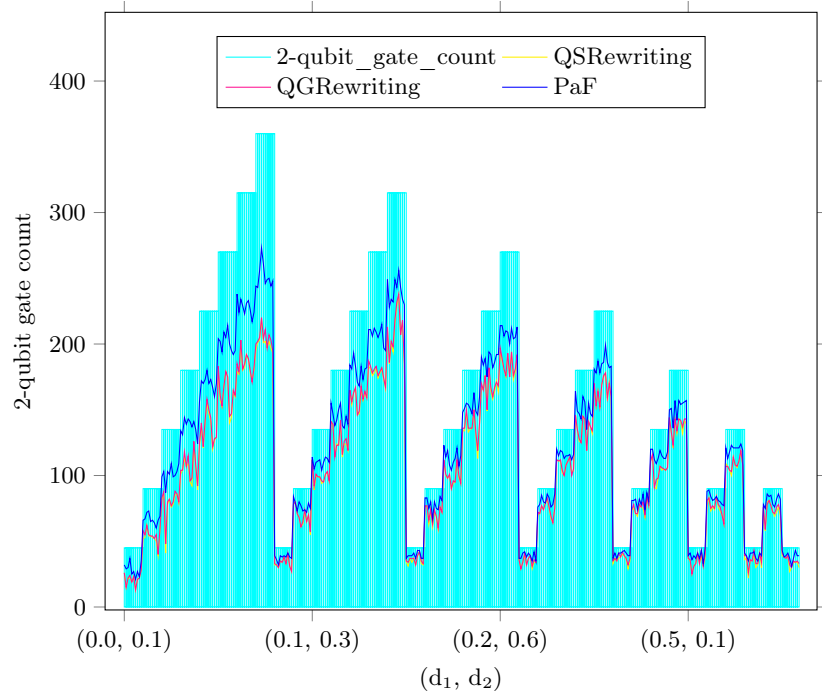
QGRewriting and PaF in terms of 1-qubit gates, 2-qubit gates, the total gate counts and depths of the optimized circuits. The cyan bar represents the gate count (depth) of the benchmarks. The blue, red, and yellow colors are for PaF, QGRewriting, and QSRewriting, respectively. We can see that the red and yellow lines are mostly lower than the blue, the yellow is mostly obscured by the red, but we can still see that it is lower than the red in some places. In Fig. 10 (d), we can see that in a few cases the depth of the quantum circuit might increase after some circuits are optimized. The reason is that the gates of a rear layer may be moved to a front layer, causing the original gate of the front layer to conflict with it.

Now we rewrite the Arithmetic and Toffoli benchmarks [22], which contain 33 circuits and 201554 gates, from the G_{IBM} gate set to the G_{Sur} gate set (cf. Table 1). The Surface-17 processor limits 1-qubit gates to X and Y rotations, and more specifically $\pm\frac{\pi}{4}$, $\pm\frac{\pi}{2}$, and $\pm\pi$ degrees will be used in our decomposition. The primitive 2-qubit gate on this processor is CZ [17]. In this experiment, we simply choose the greedy policy since no replacement conflict arises.

In Tables 3 and 4, we list the experimental data. Comparing the circuit rewriting with and without internal optimization, the gate count is reduced by up to 52%, and the depth is reduced by up to 49%. However, there is a price to pay. For a quantum circuit with millions of instructions, a rewriting without optimization takes about 15 minutes, while a rewriting with optimization may take about two hours, depending on the size of the internal rule library.



(a)



(b)

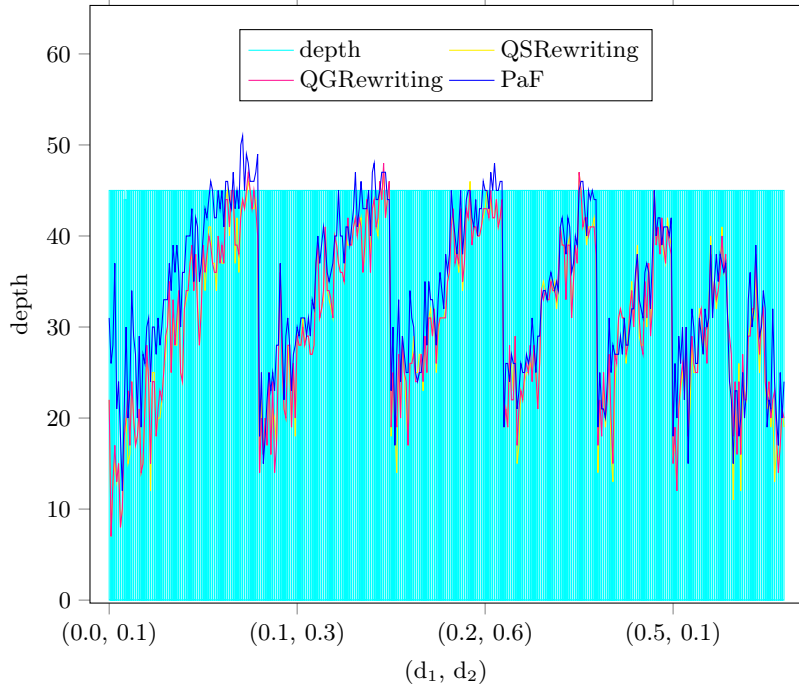
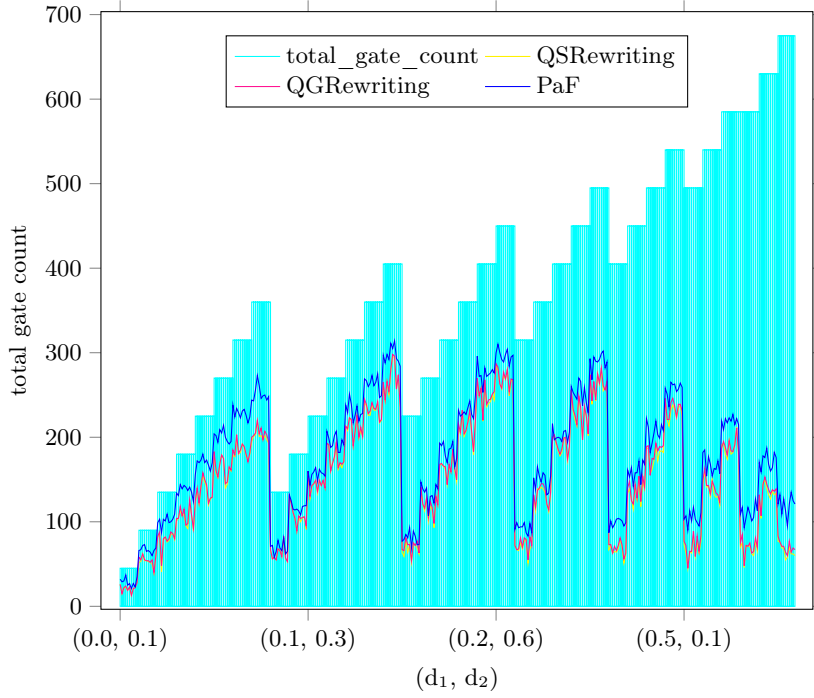


Fig. 10: Comparison of the 1-qubit gate, 2-qubit gate, total gate counts, and depths of the quantum circuits generated by QSRewriting, QGRewriting and PaF.

Table 3: Comparison of the gate counts of circuits.

benchmark	n	g	g_0	t_0	g_1	t_1	g_2	t_2	Δ
Toff-NC ₃	5	9	45	0.00	135	0.03	80	0.50	40.74%
Toff-Barenc ₃	5	10	58	0.00	174	0.07	101	0.52	41.95%
Mod 5 ₄	5	15	63	0.00	187	0.09	89	0.57	52.41%
Toff-NC ₄	7	15	75	0.00	225	0.10	134	0.89	40.44%
Toff-Barenc ₄	7	18	114	0.00	342	0.19	198	1.12	42.11%
Toff-NC ₅	9	21	105	0.00	315	0.18	188	1.34	40.32%
Toff-Barenc ₅	9	26	170	0.01	510	0.32	296	1.70	41.96%
VBE-Adder ₃	10	30	150	0.00	450	0.34	266	1.51	40.89%
GF(2 ⁴)-Mult	12	33	225	0.01	675	0.58	388	2.68	42.52%
Mod-Mult ₅₅	9	35	119	0.00	341	0.20	211	1.04	38.12%
GF(2 ⁵)-Mult	15	47	347	0.01	1041	0.80	601	3.74	42.27%
CSLA-MUX ₃	15	50	170	0.01	510	0.44	315	2.23	38.24%
Toff-NC ₁₀	19	51	255	0.01	765	0.49	458	3.31	40.13%
GF(2 ⁶)-Mult	18	63	495	0.02	1485	1.19	854	5.36	42.49%
Toff-Barenc ₁₀	19	66	450	0.01	1350	0.95	786	4.76	41.78%
RC-Adder ₆	14	68	200	0.01	584	0.93	361	2.66	38.18%
Mod-Red ₂₁	11	74	278	0.01	786	0.93	463	3.39	41.09%
GF(2 ⁷)-Mult	21	81	669	0.02	2007	1.61	1153	7.37	42.55%
CSUM-MUX ₉	30	84	420	0.01	1204	1.57	721	3.98	40.12%
QCLA-Com ₇	24	95	443	0.01	1299	1.02	778	5.98	40.11%
QCLA-Adder ₁₀	36	113	521	0.01	1563	1.31	957	7.29	38.77%
GF(2 ⁸)-Mult	24	115	883	0.02	2649	2.35	1516	12.95	42.77%
GF(2 ⁹)-Mult	27	123	1095	0.03	3285	2.72	1885	12.09	42.62%
GF(2 ¹⁰)-Mult	30	147	1347	0.03	4041	3.36	2316	14.90	42.69%
QCLA-Mod ₇	26	176	884	0.02	2638	2.06	1570	12.24	40.49%
Adder ₈	24	216	900	0.02	2676	6.79	1623	13.00	39.35%
GF(2 ¹⁶)-Mult	48	363	3435	0.13	10305	9.44	5865	38.96	43.09%
Mod-Adder ₁₀₂₄	28	865	4285	0.09	12855	18.19	7403	57.77	42.41%
GF(2 ³²)-Mult	96	1305	13593	0.30	40779	38.71	23069	157.25	43.43%
GF(2 ⁶⁴)-Mult	192	4539	53691	1.17	161073	146.63	91065	635.20	43.46%
GF(2 ¹²⁸)-Mult	384	17275	213883	5.59	641649	584.97	362429	3656.48	43.52%
GF(2 ¹³¹)-Mult	393	18333	224265	5.90	672795	616.90	379766	3927.99	43.55%
GF(2 ¹⁶³)-Mult	489	27705	346533	9.67	1039599	945.51	587034	7452.82	43.53%

Note: n : the number of qubits. g : the gate count of the target circuit. g_0 : the gate count of the target circuit after decomposition without internal optimization on G_{IBM} gate set. g_1 : the gate count of the target circuit without internal optimization on G_{Sur} gate set. g_2 : the gate count of the target circuit with internal optimization on G_{Sur} gate set. $t_0 - t_2$: running time in seconds. Δ : $(g_1 - g_2)/g_1 \times 100\%$.

Table 4: Comparison of the depths of circuits.

benchmark	n	d	d_0	t_0	d_1	t_1	d_2	t_2	Δ
Toff-NC ₃	5	7	23	0.00	64	0.03	42	0.50	34.38%
Toff-Barenc ₃	5	9	31	0.00	86	0.07	52	0.52	39.53%
Mod 5 ₄	5	15	36	0.00	97	0.09	49	0.57	49.48%
Toff-NC ₄	7	11	38	0.00	104	0.10	67	0.89	35.58%
Toff-Barenc ₄	7	17	61	0.00	166	0.19	102	1.12	38.55%
Toff-NC ₅	9	15	53	0.00	144	0.18	92	1.34	36.11%
Toff-Barenc ₅	9	25	91	0.01	246	0.32	152	1.70	38.21%
VBE-Adder ₃	10	20	70	0.00	194	0.34	113	1.51	41.75%
GF(2 ⁴)-Mult	12	17	85	0.01	236	0.58	145	2.68	38.56%
Mod-Mult ₅₅	9	14	43	0.00	118	0.20	80	1.04	32.20%
GF(2 ⁵)-Mult	15	20	111	0.01	310	0.80	187	3.74	39.68%
CSLA-MUX ₃	15	17	59	0.01	166	0.44	107	2.23	35.54%
Toff-NC ₁₀	19	35	128	0.01	344	0.49	217	3.31	36.92%
GF(2 ⁶)-Mult	18	25	139	0.02	384	1.19	235	5.36	38.80%
Toff-Barenc ₁₀	19	65	241	0.01	646	0.95	402	4.76	37.77%
RC-Adder ₆	14	28	93	0.01	261	0.93	166	2.66	36.40%
Mod-Red ₂₁	11	43	141	0.01	383	0.93	238	3.39	37.86%
GF(2 ⁷)-Mult	21	29	166	0.02	458	1.61	280	7.37	38.86%
CSUM-MUX ₉	30	15	53	0.01	147	1.57	96	3.98	34.69%
QCLA-Com ₇	24	15	70	0.01	192	1.02	115	5.98	40.10%
QCLA-Adder ₁₀	36	15	64	0.01	182	1.31	111	7.29	39.01%
GF(2 ⁸)-Mult	24	39	199	0.02	544	2.35	335	12.95	38.42%
GF(2 ⁹)-Mult	27	36	219	0.03	606	2.72	367	12.09	39.44%
GF(2 ¹⁰)-Mult	30	40	246	0.03	680	3.36	412	14.90	39.41%
QCLA-Mod ₇	26	39	172	0.02	487	2.06	284	12.24	41.68%
Adder ₈	24	55	191	0.02	527	6.79	315	13.00	40.23%
GF(2 ¹⁶)-Mult	48	71	415	0.13	1136	9.44	699	38.96	38.47%
Mod-Adder ₁₀₂₄	28	521	2218	0.09	6397	18.19	3775	57.77	40.99%
GF(2 ³²)-Mult	96	137	849	0.30	2324	38.71	1447	157.25	37.74%
GF(2 ⁶⁴)-Mult	192	263	1711	1.17	4688	146.63	2856	635.20	39.08%
GF(2 ¹²⁸)-Mult	384	517	3437	5.59	9420	584.97	5750	3656.48	38.96%
GF(2 ¹³¹)-Mult	393	537	3526	5.90	9658	616.90	5902	3927.99	38.89%
GF(2 ¹⁶³)-Mult	489	665	4390	9.67	12026	945.51	7310	7452.82	39.22%

Note: n : the number of qubits. d : the depth of the target circuit. d_0 : the depth of the target circuit after decomposition without internal optimization on G_{IBM} gate set. d_1 : the depth of the rewritten circuit without internal optimization on G_{Sur} gate set. d_2 : the depth of the rewritten circuit with internal optimization on G_{Sur} gate set. $t_0 - t_2$: running time in seconds. Δ : $(d_1 - d_2)/d_1 \times 100\%$.

8 Conclusion

We introduced a new representation of quantum circuits, which reduced the pattern matching of circuits to the problem of finding distinct subsequences. We presented an algorithm based on dynamic programming to match the pattern circuits in the target circuit. To resolve replacement conflicts, we proposed three policies for generating replacement schedulers and a polynomial-time replacement algorithm. We developed a rule library for basic optimizations and applied it to rewrite the Arithmetic and Toffoli benchmarks from the G_{IBM} gate set to the G_{Sur} gate set. Compared with the existing tool PaF, QRewriting improved the depth (resp. gate count) reduction by 29% (resp. 14%), which demonstrated the effectiveness of our approach.

References

1. Abdessaied, N., Soeken, M., Wille, R., Drechsler, R.: Exact template matching using boolean satisfiability. In: 2013 IEEE 43rd International Symposium on Multiple-Valued Logic. pp. 328–333 (2013)
2. Amy, M., Azimzadeh, P., Mosca, M.: On the controlled-NOT complexity of controlled-NOT-phase circuits. *Quantum Science and Technology* **4**(1), 015002 (2018)
3. Arute, F., Arya, K., et al.: Quantum supremacy using a programmable superconducting processor. *Nature* **574**, 505–510 (2019)
4. Ball, P.: First quantum computer to pack 100 qubits enters crowded race. *Nature* **599**, 542 (2021)
5. Bellman, R.E.: *Dynamic Programming*. Dover Publications, Inc., USA (2003)
6. Chen, M., Zhang, Y., Li, Y.: A quantum circuit optimization framework based on pattern matching. *SPIN* **11**(03), 2140008 (2021)
7. Dumitrescu, E., McCaskey, A., Hagen, G., Jansen, G., Morris, T., Papenbrock, T., Pooser, R., Dean, D., Lougovski, P.: Cloud quantum computing of an atomic nucleus. *Physical Review Letters* **120**(21) (may 2018)
8. Grover, L.K.: A fast quantum mechanical algorithm for database search. In: Proc. 28th Annual ACM Symposium on the Theory of Computing. pp. 212–219. ACM (1996)
9. Harrow, A.W., Hassidim, A., Lloyd, S.: Quantum algorithm for solving linear systems of equations. *Physical Review Letters* **103**(15), 150502 (2009)
10. IBM: Qiskit: An open-source SDK for working with quantum computers at the level of pulses, circuits, and algorithms. <https://github.com/QISKit> (2020)
11. Iten, R., Moyard, R., Metger, T., Sutter, D., Woerner, S.: Exact and practical pattern matching for quantum circuit optimization (2020)
12. Iwama, K., Kambayashi, Y., Yamashita, S.: Transformation rules for designing cnot-based quantum circuits. In: Proceedings of the 39th Annual Design Automation Conference. p. 419–424. Association for Computing Machinery (2002)
13. Jia, Z., Padon, O., Thomas, J., Warszawski, T., Zaharia, M., Aiken, A.: Taso: Optimizing deep learning computation with automatic generation of graph substitutions. In: Proceedings of the 27th ACM Symposium on Operating Systems Principles. p. 47–62. Association for Computing Machinery, New York, NY, USA (2019)

14. Kissinger, A., van de Wetering, J.: PyZX: Large scale automated diagrammatic reasoning. *Electronic Proceedings in Theoretical Computer Science* **318**, 229–241 (may 2020)
15. Kjaergaard, M., Schwartz, M.E., Braumüller, J., Krantz, P., Wang, J.I.J., Gustavsson, S., Oliver, W.D.: Superconducting qubits: Current state of play. *Annual Review of Condensed Matter Physics* **11**(1), 369–395 (2020)
16. Kjaergaard, M., Schwartz, M.E., Braumüller, J., Krantz, P., Wang, J.I.J., Gustavsson, S., Oliver, W.D.: Superconducting qubits: Current state of play. *Annual Review of Condensed Matter Physics* **11**(1), 369–395 (2020)
17. Lao, L., van Someren, H., Ashraf, I., Almudéver, C.G.: Timing and resource-aware mapping of quantum circuits to superconducting processors. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **41**(2), 359–371 (2022)
18. Liu, J., Bello, L., Zhou, H.: Relaxed peephole optimization: A novel compiler optimization for quantum circuits. In: 2021 IEEE/ACM International Symposium on Code Generation and Optimization. pp. 301–314 (2021)
19. Madsen, L.S., Laudendach, F., Askarani, M.F., Rortais, F., Vincent, T., Bulmer, J.F.F., Miatto, F.M., Neuhaus, L., Helt, L.G., Collins, M.J., Lita, A.E., Gerrits, T., Nam, S.W., Vaidya, V.D., Menotti, M., Dhand, I., Vernon, Z., Quesada, N., Lavoie, J.: Quantum computational advantage with a programmable photonic processor. *Nature* **606**, 75–81 (2022)
20. McKeeman, W.M.: Peephole optimization. *Commun. ACM* **8**(7), 443–444 (1965)
21. Murali, P., Linke, N.M., Martonosi, M., Abhari, A.J., Nguyen, N.H., Alderete, C.H.: Full-stack, real-system quantum computer studies: Architectural comparisons and design insights. In: 2019 ACM/IEEE 46th Annual International Symposium on Computer Architecture (ISCA). pp. 527–540 (2019)
22. Nam, Y.S., Ross, N.J., Su, Y., Childs, A.M., Maslov, D.: Automated optimization of large quantum circuits with continuous parameters. *npj Quantum Information* **4**, 23 (2018)
23. Nielsen, M.A., Chuang, I.L.: *Quantum Computation and Quantum Information* (10th Anniversary edition). Cambridge University Press (2016)
24. Pointing, J., Padon, O., Jia, Z., Ma, H., Hirth, A., Palsberg, J., Aiken, A.: *Quanto: Optimizing quantum circuits with automatic generation of circuit identities* (2021)
25. Prasad, A.K., Shende, V.V., Markov, I.L., Hayes, J.P., Patel, K.N.: Data structures and algorithms for simplifying reversible circuits. *ACM J. Emerg. Technol. Comput. Syst.* **2**(4), 277–293 (2006)
26. Preskill, J.: Quantum Computing in the NISQ era and beyond. *Quantum* **2**, 79 (Aug 2018)
27. Rahman, M.M., Dueck, G.W.: Optimal quantum circuits of three qubits. In: 2012 IEEE 42nd International Symposium on Multiple-Valued Logic. pp. 161–166 (2012)
28. Shor, P.W.: Algorithms for quantum computation: Discrete logarithms and factoring. In: Proc. 35th Annual Symposium on Foundations of Computer Science. pp. 124–134. IEEE Computer Society (1994)
29. Sivaram, S., Dilkes, S., Cowtan, A., Simmons, W., Edgington, A., Duncan, R.: `t|ket>`: a retargetable compiler for NISQ devices. *Quantum Science and Technology* **6**(1), 014003 (nov 2020)
30. Skilbeck, M., Peterson, E., Appleby, Davis, E., Karalekas, P., Bello-Rivas, J.M., Kochmanski, D., Beane, Z., Smith, R., Shi, A., Scott, C., Paszke, A., Hulburd, E., Young, M., Jackson, A.S., BHAVISHYA, Alam, M.S., Velázquez-Rodríguez, W., c. b. osborn, fengdlm, jmackeyrigetti: `rigetti/quilc: v1.21.0` (Jul 2020)

31. Soeken, M., Dueck, G.W., Rahman, M.M., Miller, D.M.: An extension of transformation-based reversible and quantum circuit synthesis. In: 2016 IEEE International Symposium on Circuits and Systems (ISCAS). pp. 2290–2293 (2016)
32. Tan, B., Cong, J.: Optimality study of existing quantum computing layout synthesis tools. *IEEE Transactions on Computers* (Jul 2020)
33. Xu, M., Li, Z., Padon, O., Lin, S., Pointing, J., Hirth, A., Ma, H., Palsberg, J., Aiken, A., Acar, U.A., Jia, Z.: Quartz: Superoptimization of quantum circuits. In: Proceedings of the 43rd ACM SIGPLAN Conference on Programming Language Design and Implementation (2022)
34. Zhang, Y., Deng, H., Li, Q., Song, H., Nie, L.: Optimizing quantum programs against decoherence: Delaying qubits into quantum superposition. In: 2019 International Symposium on Theoretical Aspects of Software Engineering. pp. 184–191. IEEE (2019)